

**HALF-BRIDGE DRIVER**

**Features**

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Shut down input turns off both channels
- Matched propagation delay for both channels
- Also available LEAD-FREE

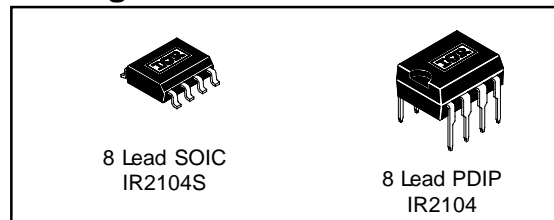
**Description**

The IR2104(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

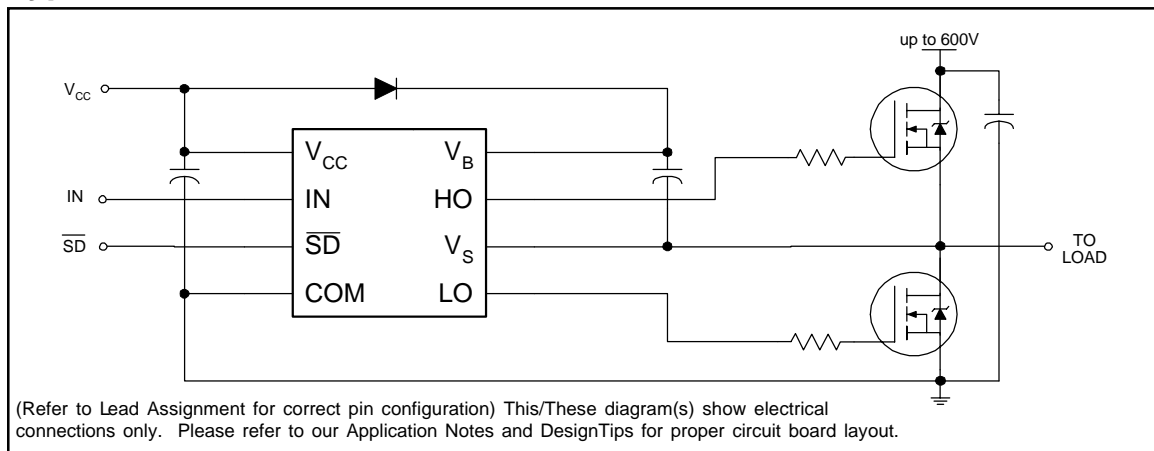
**Product Summary**

$V_{\text{OFFSET}}$	600V max.
$I_{\text{O}+/-}$	130 mA / 270 mA
$V_{\text{OUT}}$	10 - 20V
$t_{\text{on/off (typ.)}}$	680 & 150 ns
Deadtime (typ.)	520 ns

**Packages**



**Typical Connection**



# IR2104(S)&(PbF)

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating absolute voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (IN & $\overline{SD}$ )	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (IN & $\overline{SD}$ )	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

### Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	680	820	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	150	220		$V_S = 600V$
$t_{sd}$	Shutdown propagation delay	—	160	220		
$t_r$	Turn-on rise time	—	100	170		
$t_f$	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

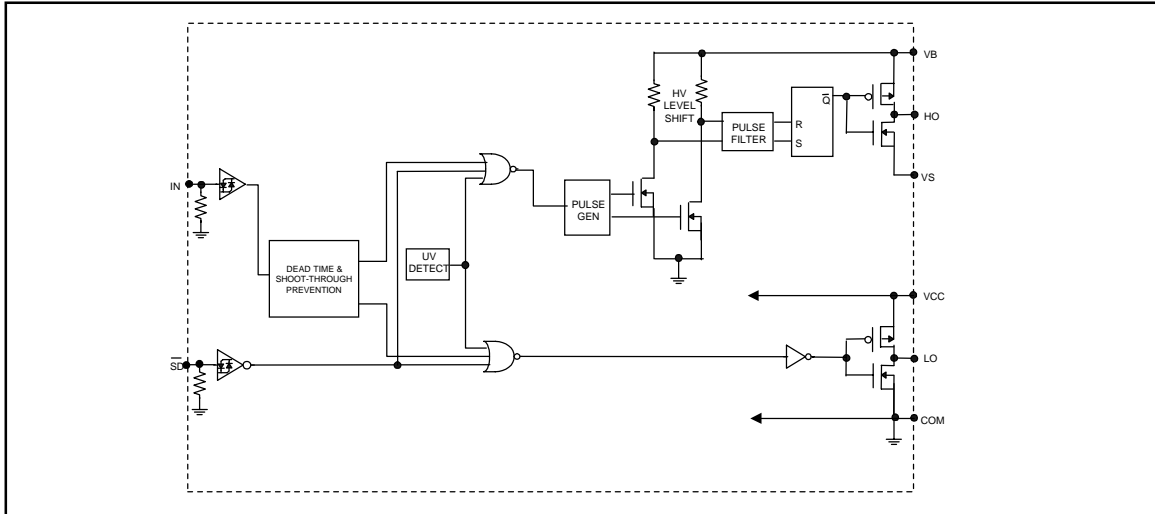
### Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" (HO) & Logic "0" (LO) input voltage	3	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" (HO) & Logic "1" (LO) input voltage	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{SD,TH+}$	SD input positive going threshold	3	—	—		$V_{CC} = 10V$ to 20V
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low level output voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	30	55		$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	150	270		$V_{IN} = 0V$ or 5V
$I_{IN+}$	Logic "1" input bias current	—	3	10		$V_{IN} = 5V$
$I_{IN-}$	Logic "0" input bias current	—	—	1		$V_{IN} = 0V$
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8	8.9	9.8	V	
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9		
$I_{O+}$	Output high short circuit pulsed current	130	210	—	mA	$V_O = 0V$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	270	360	—		$V_O = 15V$ $PW \leq 10 \mu s$

# IR2104(S)&(PbF)

## Functional Block Diagram



## Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
$\overline{SD}$	Logic input for shutdown
$V_B$	High side floating supply
HO	High side gate drive output
$V_S$	High side floating supply return
$V_{CC}$	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

<p>8 Lead PDIP</p>	<p>8 Lead SOIC</p>
<b>IR2104</b>	<b>IR2104S</b>

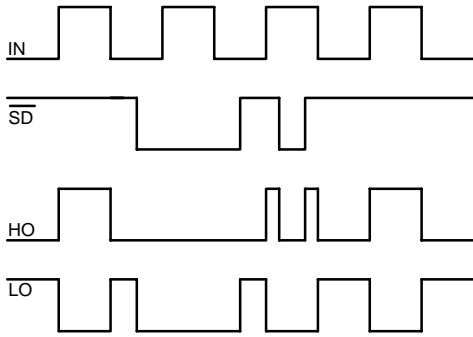


Figure 1. Input/Output Timing Diagram

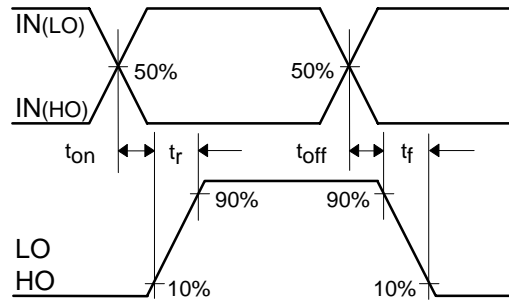


Figure 2. Switching Time Waveform Definitions

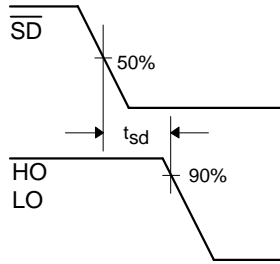


Figure 3. Shutdown Waveform Definitions

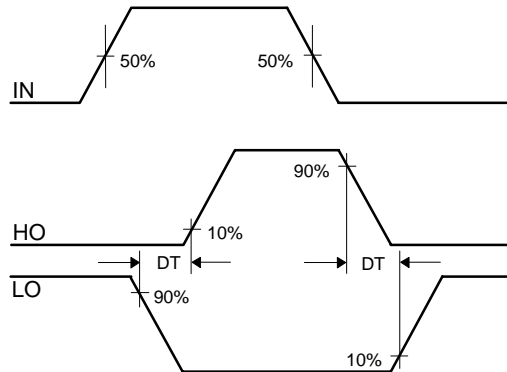


Figure 4. Deadtime Waveform Definitions

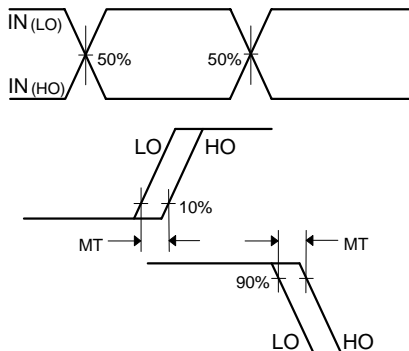


Figure 5. Delay Matching Waveform Definitions

# IR2104(S)&(PbF)

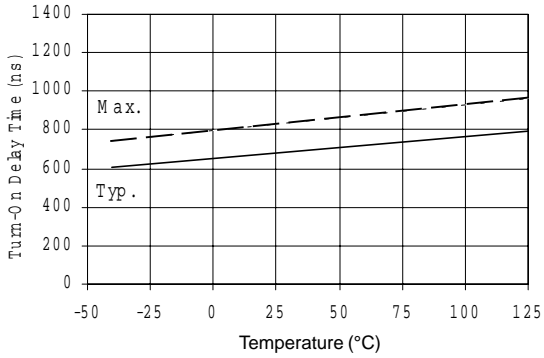


Figure 6A. Turn-On Time vs Temperature

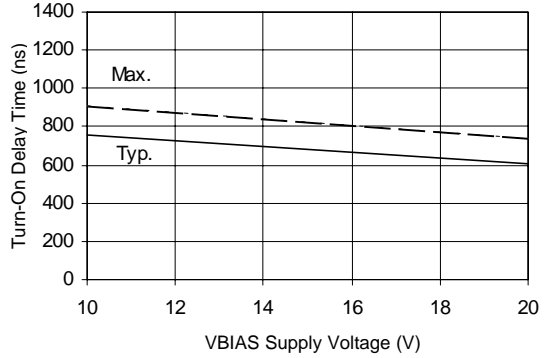


Figure 6B. Turn-On Time vs Supply Voltage

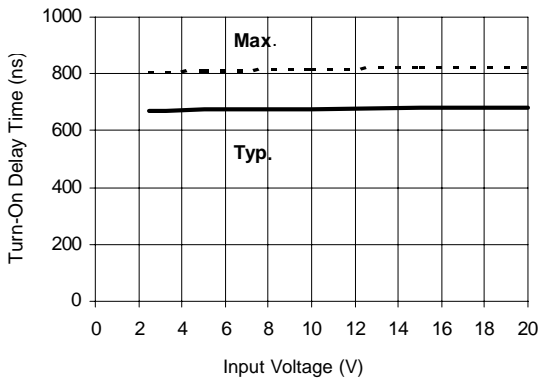


Figure 6C. Turn-On Time vs Input Voltage

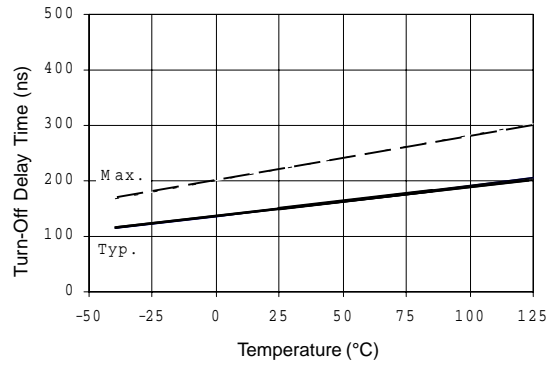


Figure 7A. Turn-Off Time vs Temperature

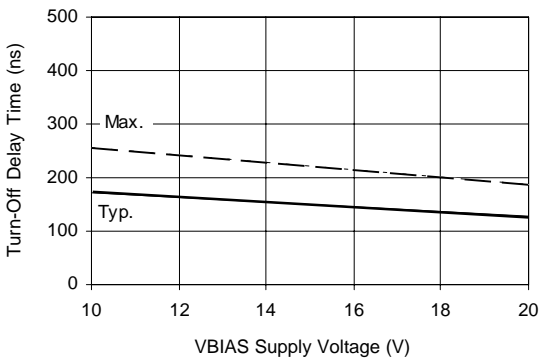


Figure 7B. Turn-Off Time vs Supply Voltage

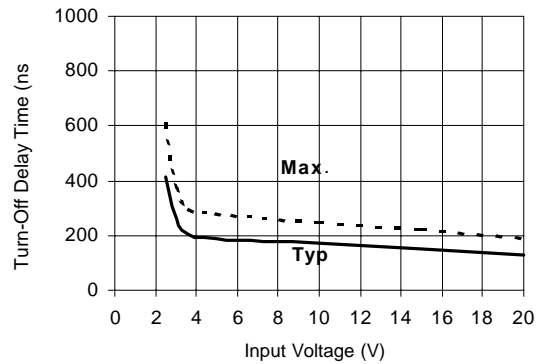
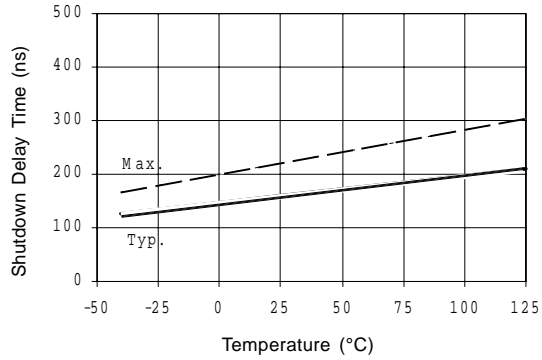
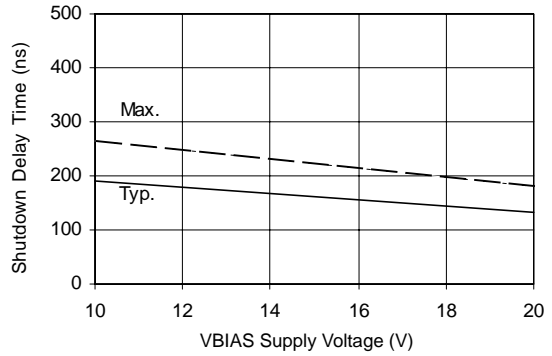


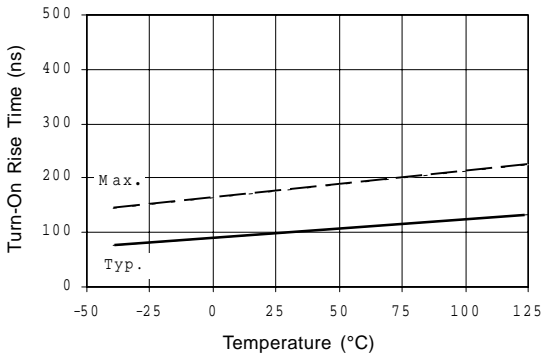
Figure 7C. Turn-Off Time vs Input Voltage



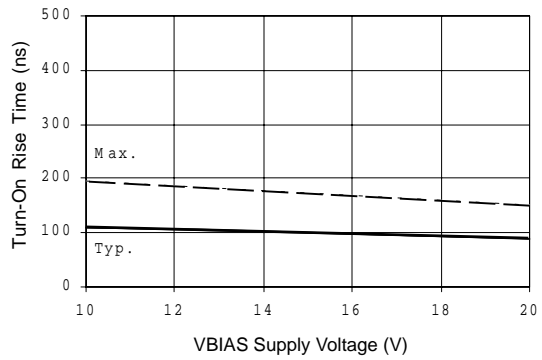
**Figure 8A. Shutdown Time vs Temperature**



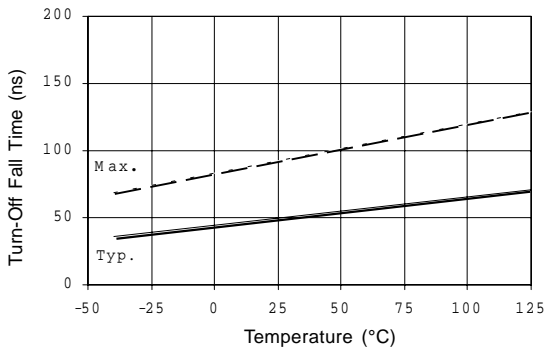
**Figure 8B. Shutdown Time vs Voltage**



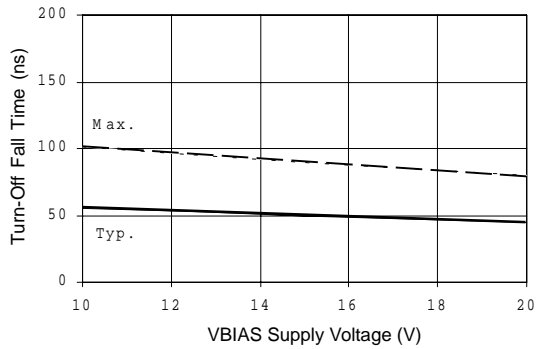
**Figure 9A. Turn-On Rise Time vs Temperature**



**Figure 9B. Turn-On Rise Time vs Voltage**



**Figure 10A. Turn-Off Fall Time vs Temperature**



**Figure 10B. Turn-Off Fall Time vs Voltage**

# IR2104(S)&(PbF)

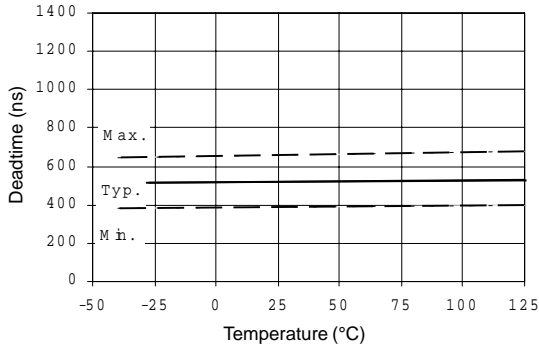


Figure 11A. Deadtime vs Temperature

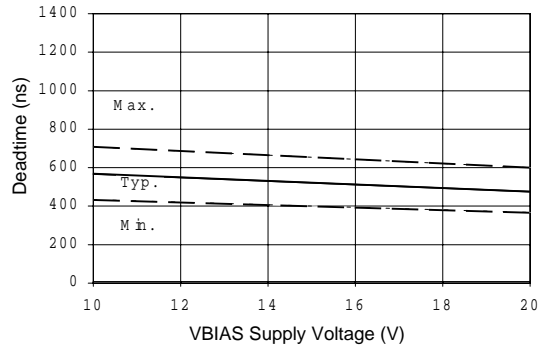


Figure 11B. Deadtime vs Voltage

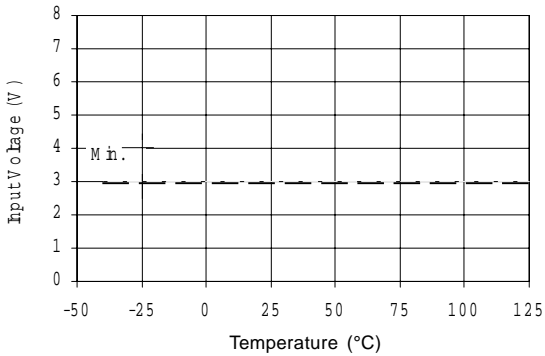


Figure 12A. Logic "1" (HO) & Logic "0" (LO) & Inactive SD Input Voltage vs Temperature

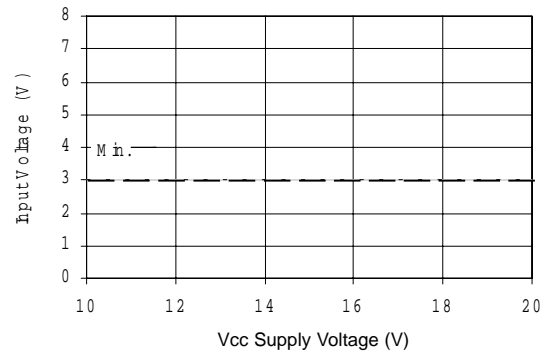


Figure 12B. Logic "1" (HO) & Logic "0" (LO) & Inactive SD Input Voltage vs Voltage

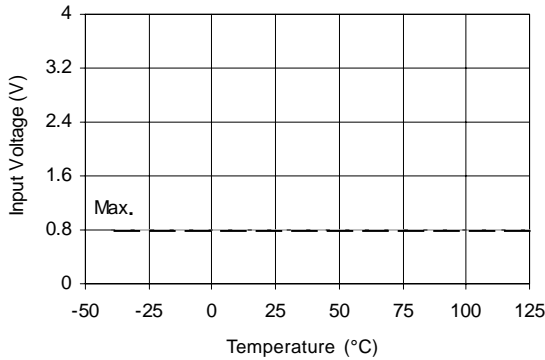


Figure 13A. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs Temperature

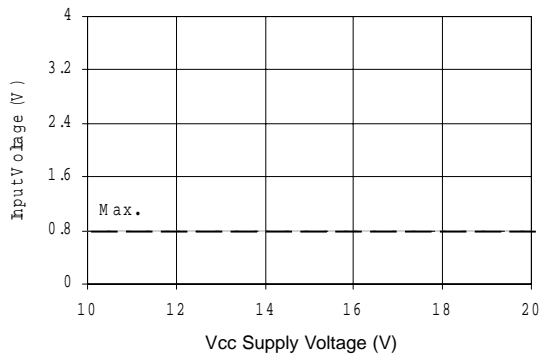
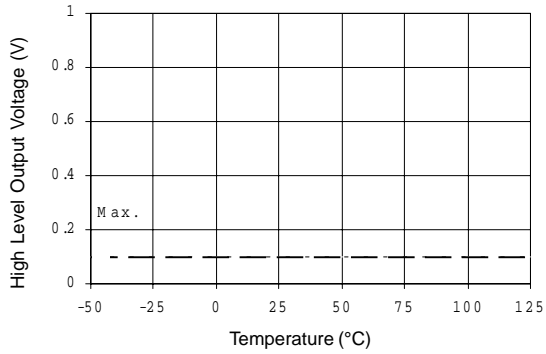
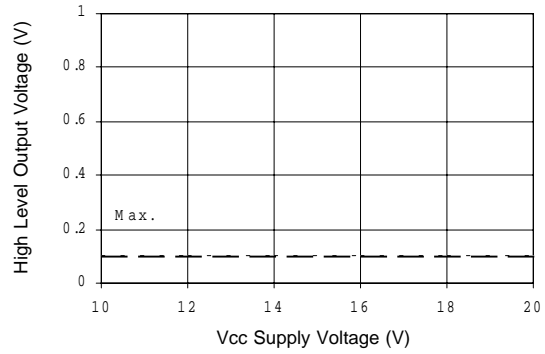


Figure 13B. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs Voltage

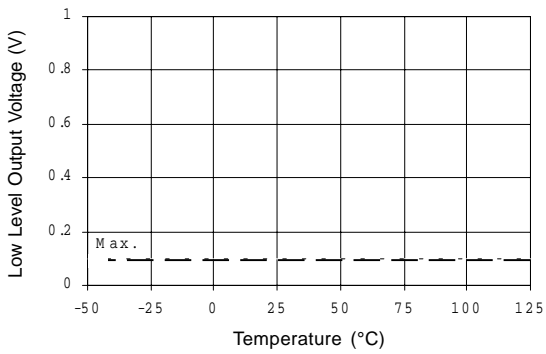




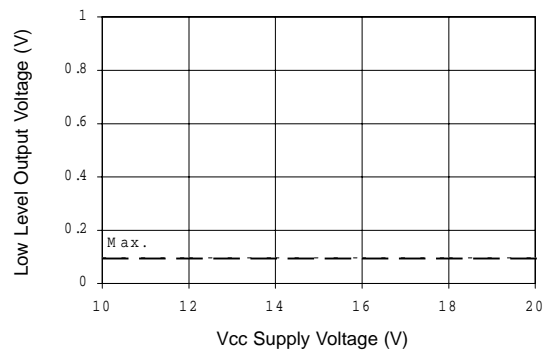
**Figure 14A. High Level Output vs Temperature**



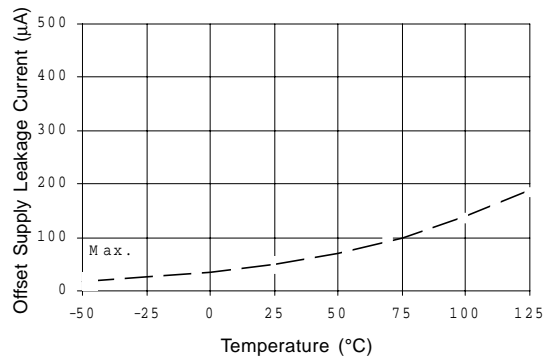
**Figure 14B. High Level Output vs Voltage**



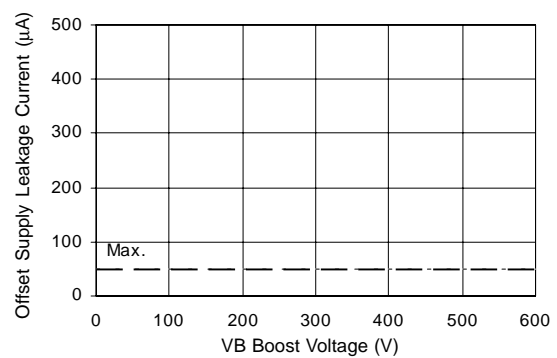
**Figure 15A. Low Level Output vs Temperature**



**Figure 15B. Low level Output vs Voltage**

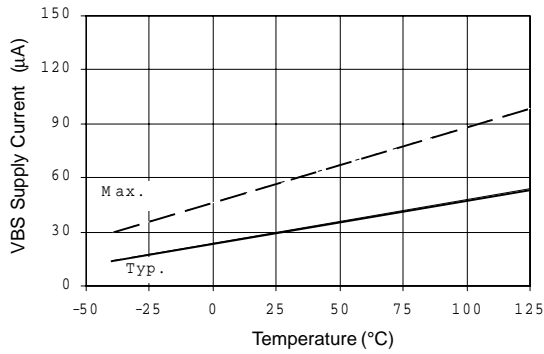


**Figure 16A. Offset Supply Current vs Temperature**

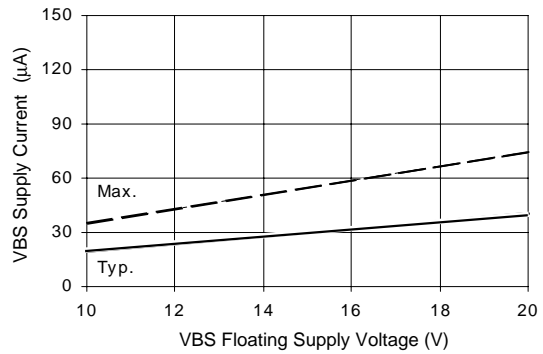


**Figure 16B. Offset Supply Current vs Voltage**

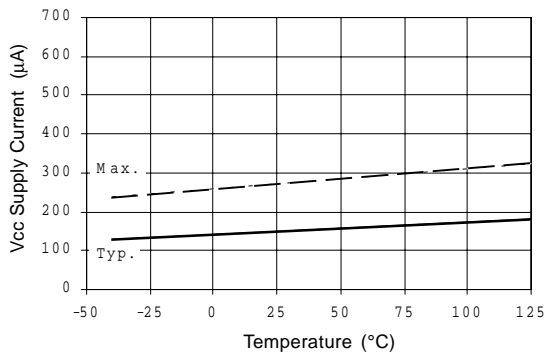
# IR2104(S)&(PbF)



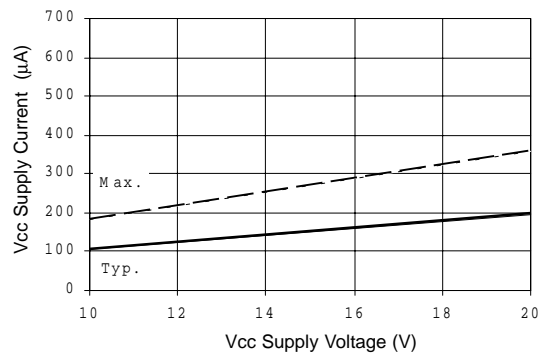
**Figure 17A. VBS Supply Current vs Temperature**



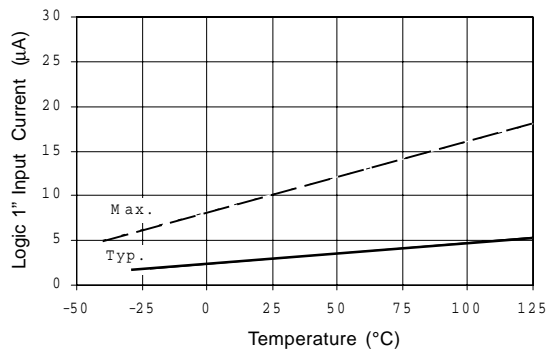
**Figure 17B. VBS Supply Current vs Voltage**



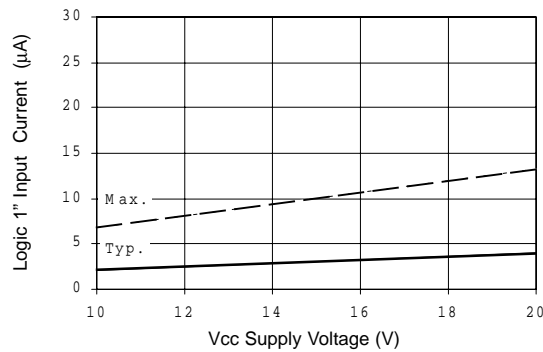
**Figure 18A. VCC Supply Current vs Temperature**



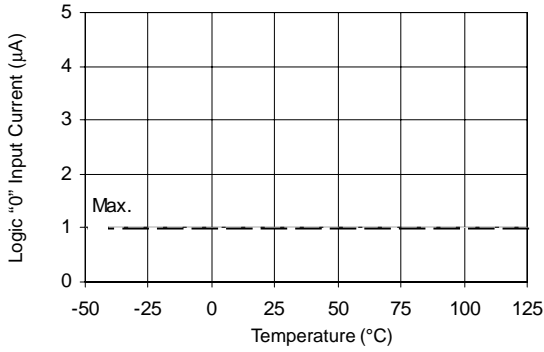
**Figure 18B. VCC Supply Current vs Voltage**



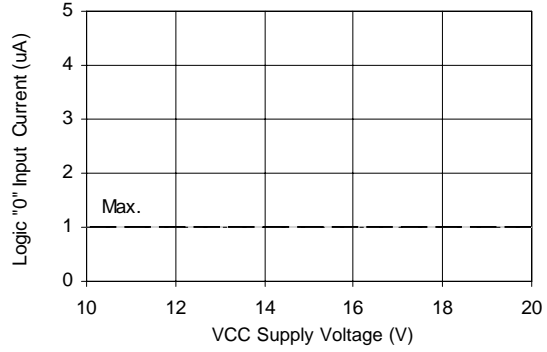
**Figure 19A. Logic "1" Input Current vs Temperature**



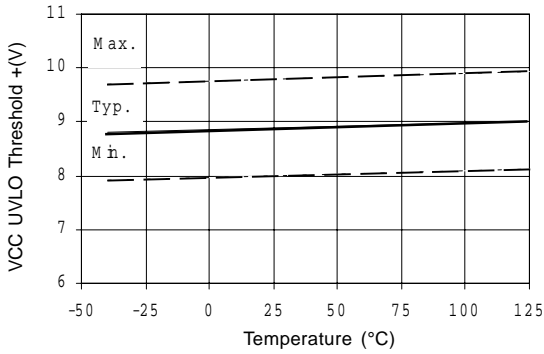
**Figure 19B. Logic "1" Input Current vs Voltage**



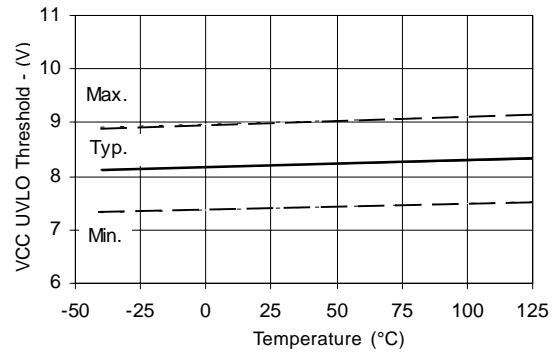
**Figure 20A. Logic "0" Input Current vs Temperature**



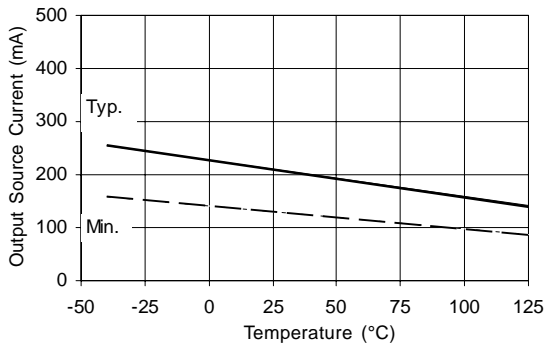
**Figure 20B. Logic "0" Input Current vs Voltage**



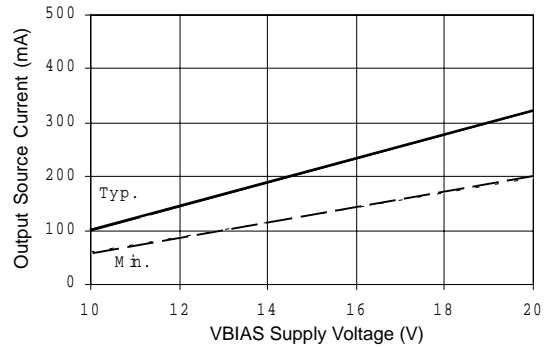
**Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature**



**Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature**

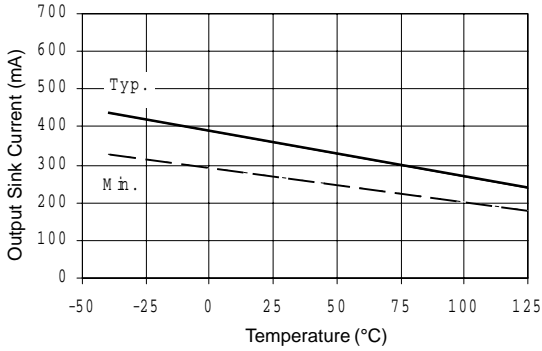


**Figure 22A. Output Source Current vs Temperature**

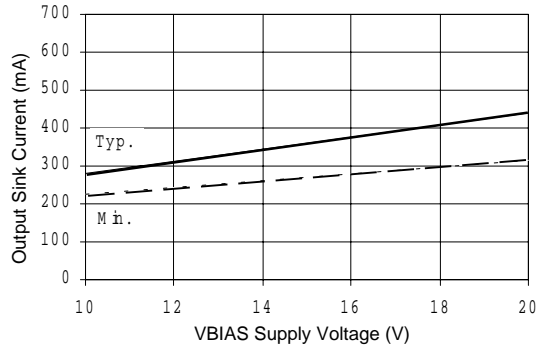


**Figure 22B. Output Source Current vs Voltage**

# IR2104(S)&(PbF)

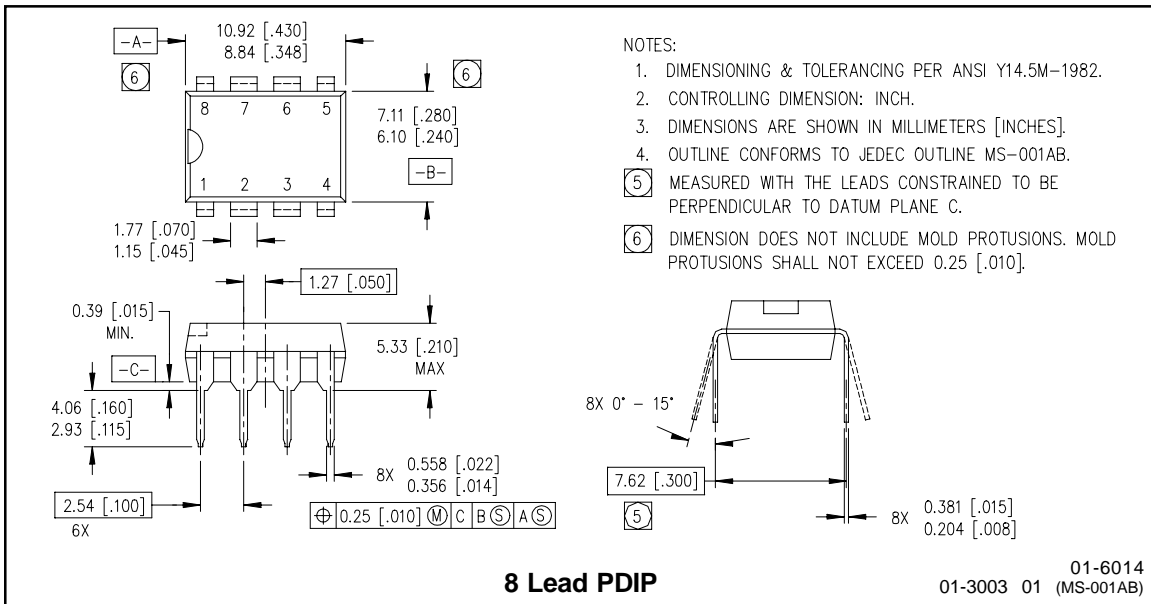


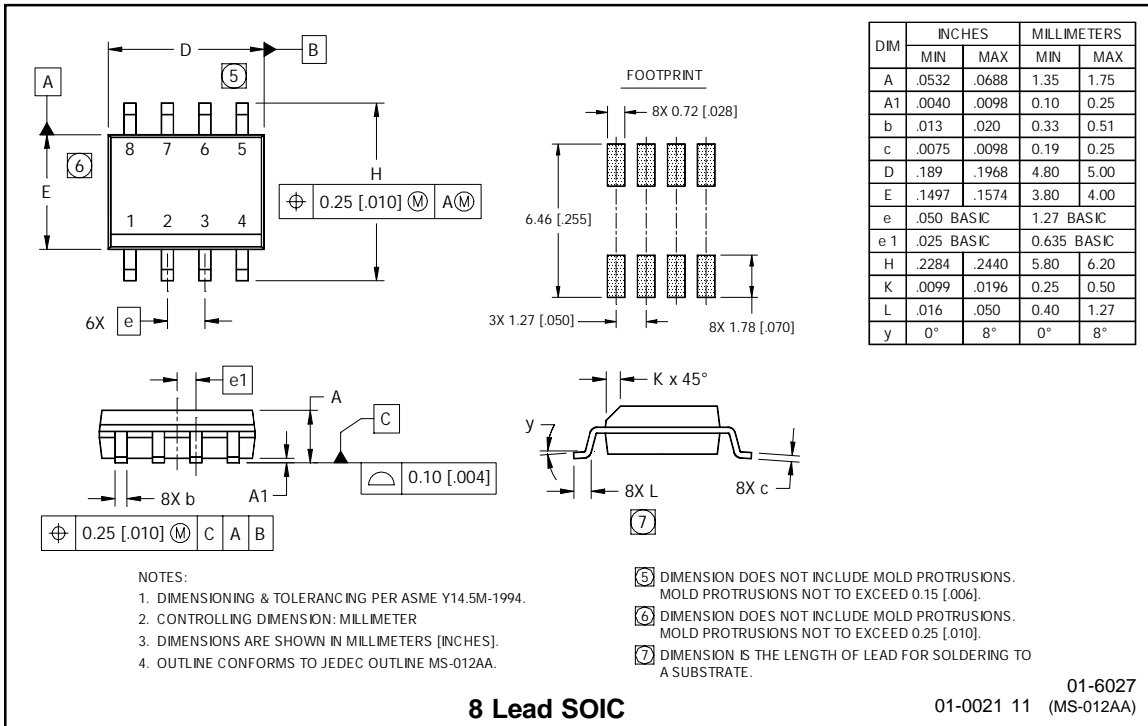
**Figure 23A. Output Sink Current vs Temperature**



**Figure 23B. Output Sink Current vs Voltage**

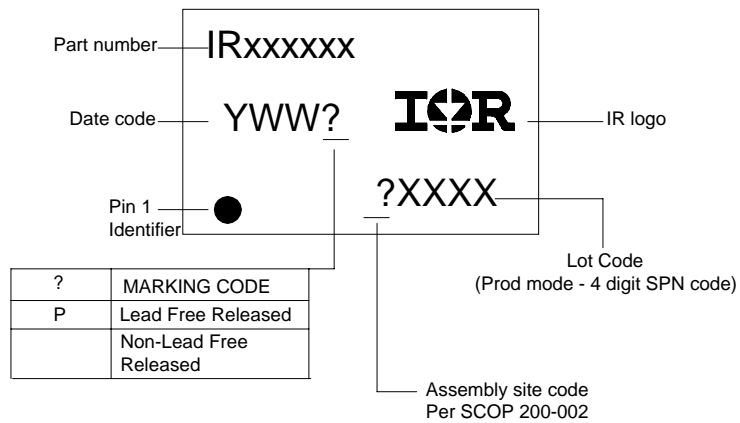
## Case Outlines





# IR2104(S)&(PbF)

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

8-Lead PDIP IR2104 order IR2104  
8-Lead SOIC IR2104S order IR2104S

### Leadfree Part

8-Lead PDIP IR2104 order IR2104PbF  
8-Lead SOIC IR2104S order IR2104SPbF