International
IOR Rectifier

Data Sheet No. PD94710

IR3082

XPHASE™ AMD OPTERON™/ATHLON 64™ CONTROL IC

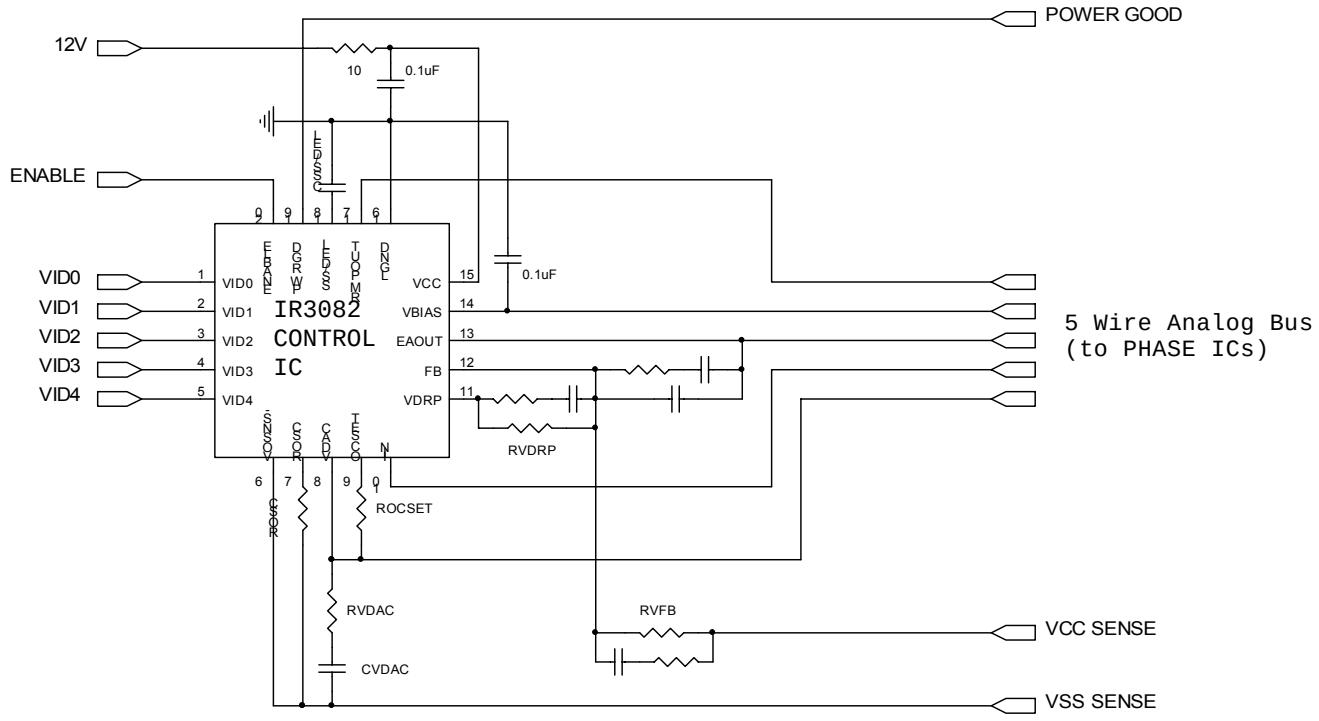
DESCRIPTION

The IR3082 Control IC combined with an IR *XPhase*™ Phase IC provides a full featured and flexible way to implement a complete Opteron or Athlon64 power solution. The "Control" IC provides overall system control and interfaces with any number of "Phase ICs" which each drive and monitor a single phase of a multiphase converter. With simple 5 bit voltage programming and a few external components, the IR3082 is also well suited for general purpose multiphase applications. The *XPhase*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- 5 bit VID with 1% overall system set point accuracy
- Programmable Dynamic VID Slew Rate
- +/-300mV Differential Remote Sense
- Programmable 150kHz to 1MHz oscillator
- Programmable VID Offset and Load Line output impedance
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Power Good output provides indication of proper operation and avoids false triggering
- Operates from 12V input with 9.75V Under-Voltage Lockout
- 7.0V/5mA Bias Regulator provides System Reference Voltage
- Small thermally enhanced 20L MLPQ package

APPLICATION CIRCUIT



ORDERING INFORAMATION

Device	Order Quantity
IR3082MTR	3000 per reel
* IR3082M	100 piece strips

* Samples only

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC standard

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1-5	VID0-4	20V	-0.3V	1mA	1mA
6	VOSNS-	0.5V	-0.5V	10mA	10mA
7	ROSC	20V	-0.5V	1mA	1mA
8	VDAC	20V	-0.3V	1mA	1mA
9	OCSET	20V	-0.3V	1mA	1mA
10	IIN	20V	-0.3V	1mA	1mA
11	VDRP	20V	-0.3V	5mA	5mA
12	FB	20V	-0.3V	1mA	1mA
13	EAOUT	10V	-0.3V	20mA	20mA
14	VBIAS	20V	-0.3V	50mA	10mA
15	VCC	20V	-0.3V	1mA	50mA
16	LGND	n/a	n/a	50mA	1mA
17	RMPOUT	20v	-0.3V	1mA	1mA
18	SS/DEL	20V	-0.3V	1mA	1mA
19	PWRGD	20V	-0.3V	1mA	20mA
20	ENABLE	20V	-0.3V	1mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 9.6V ≤ V_{CC} ≤ 16V, -0.3V ≤ VOSNS- ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, ROSC = 24KΩ, CSS/DEL = 0.1μF +/-10%

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy (Deviation from Table 1 per test circuit in Figure 1 which emulates in-VR operation)	10KΩ ≤ ROSC ≤ 91KΩ, RFB selected to provide 50mV VID offset	-1		1	%
Source Current	Includes OCSET current	101	110	119	μA
Sink Current		92	100	108	μA
VIDx Input Threshold		1.04	1.24	1.44	V
VIDx Input Bias Current	0V ≤ VID0-4 ≤ VCC	-5	0	5	μA
VIDx 11111 Blanking Delay	Measure Time till PWRGD drives low	0.5	0.7	1	μs
Error Amplifier					
Input Offset Voltage	Measure V(FB) – V(VDAC) with EAOUT tied to FB. Applies to all VID codes. Note 2.	-5	1.5	6	mV
FB Bias Current		-53.5	-51	-48.5	μA
DC Gain	Note 1	90	100	110	dB
Gain Bandwidth Product	Note 1	6	10		MHz
Corner Frequency	45 deg Phase Shift, Note 1		400		Hz
Slew Rate	Note 1	1.4	3.2	5	V/μs
Source Current		0.4	0.7	1	mA
Sink Current		0.5	0.9	1.4	mA
Max Voltage	VBIAS–VEAOUT (referenced to VBIAS)	250	375	525	mV
Min Voltage	Normal operation or Fault mode	30	125	200	mV
VDRP Buffer Amplifier					
Input Offset Voltage	V(VDRP) – V(IIN), 0.5V ≤ V(IIN) ≤ 5V	-10	-1	6	mV
Source Current	0.5V ≤ V(IIN) ≤ 5V	1.2	3.0	5.0	mA
Sink Current	0.5V ≤ V(IIN) ≤ 5V	0.2	1.4	4.1	mA
Bandwidth	Note 1	1	6		MHz
Slew Rate	Note 1		10		V/μs
IIN Bias Current		-2	-0.3	0.4	μA
VBIAS Regulator					
Output Voltage	-5mA≤ I(VBIAS) ≤ 0	6.6	7.0	7.4	V
Current Limit		-35	-20	-6	mA
Enable Input					
Threshold Voltage	ENABLE rising	1.15	1.27	1.39	V
Threshold Voltage	ENABLE falling	1.08	1.205	1.31	V
Threshold Hysteresis		40	65	90	mV
Bias Current	0V ≤ V(ENABLE) ≤ VCC	-5	0	5	μA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay (See Fig 10)		1.2	1.9	2.6	ms
Soft Start Time (See Fig 10)	VID = 1.3V (VID4-0 = 01010)	0.85	1.95	3.0	ms
PWRGD Delay (See Fig 10)	VID = 1.3V (VID4-0 = 01010)	1.0	2.0	3.0	ms
OC Delay Time		150	250	350	us
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.95	1.3	1.6	V
Charge Current		40	66	100	μA
Discharge Current		4	6	9	μA
Charge/Discharge Current Ratio		9.5	11	12.5	μA/μA
OC Discharge Current	Note 1	20	40	60	μA
Charge Voltage		3.65	3.9	4.15	V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL rising	50	70	90	mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL falling	85	115	145	mV
Delay Comparator Hysteresis		15	35	50	mV
Discharge Comparator Threshold		175	225	275	mV
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 5V	-10	0	10	mV
OCSET Bias Current		-54	-51.5	-49	μA
PWRGD Output					
Output Voltage	I(PWRGD) = 4mA		150	300	mV
Leakage Current	V(PWRGD) = 5.5V		0	10	μA
Oscillator					
Switching Frequency		450	500	550	kHz
Peak Voltage (5V typical, measured as % of VBIAS)		70	71	74	%
Valley Voltage (1V typical, measured as % of VBIAS)		10	13	15	%
VCC Under-Voltage Lockout					
Start Threshold		9.0	9.75	10.4	V
Stop Threshold		8.4	9.0	9.6	V
Hysteresis	Start – Stop	550	750	1150	mV
General					
VCC Supply Current		8	10	12.5	mA
VOSNS- Current	-0.3V ≤ VOSNS- ≤ 0.3V, All VID Codes	-4.5	-3.5	-2.5	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amp input offsets errors

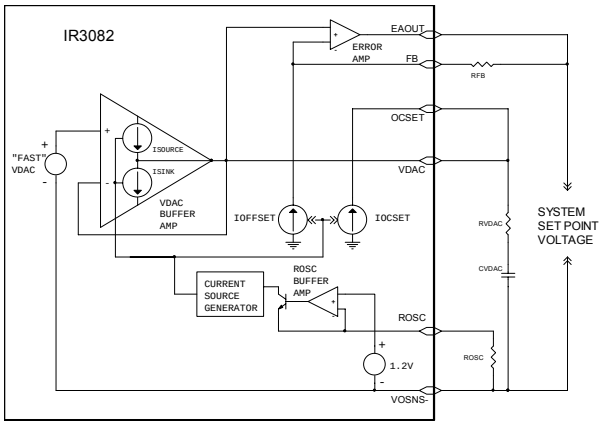


Figure 1 – System Set Point Test Circuit

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-5	VID4-0	Inputs to VID D to A Converter.
6	VOSNS-	Remote Sense Input. Connect to ground at the Load.
7	ROSC	Connect a resistor to VOSNS- to program oscillator frequency and OCSET, FB, and VDAC bias currents.
8	VDAC	Regulated voltage programmed by the VID inputs. Connect an external RC network to VOSNS- to program Dynamic VID slew rate and provide compensation for the internal Buffer Amplifier.
9	OCSET	Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source. Over-current protection can be disabled by connecting a resistor from this pin to VDAC to program the threshold higher than the possible signal into the IIN pin from the Phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
10	IIN	Current Sense input from the Phase IC(s). If current feedback from the Phase ICs is not required for implementing droop or over-current protection connect to the LGND pin. To ensure proper operation do not float this pin.
11	VDRP	Buffered IIN signal. Connect an external RC network to FB to program converter output impedance.
12	FB	Inverting input to the Error Amplifier. Converter output voltage is offset from the VDAC voltage through an external resistor connected to the converter output voltage at the load and an internal current source.
13	EAOUT	Output of the Error Amplifier.
14	VBIAS	6.8V/5mA Regulated output used as a system reference voltage for internal circuitry and the Phase ICs.
15	VCC	Power Input for internal circuitry.
16	LGND	Local Ground for internal circuitry and IC substrate connection.
17	RMPOUT	Oscillator Output voltage. Used by Phase ICs to program Phase Delay
18	SS/DEL	Controls Converter Start-up and Over-Current Timing. Connect an external capacitor to LGND to program.
19	PWRGD	Open Collector output that drives low during Start-Up and any external fault condition. Connect external pull-up.
20	ENABLE	Enable Input. A logic low applied to this pin puts the IC into Fault mode. Do not float this pin as the logic state will be undefined.

SYSTEM THEORY OF OPERATION

XPhase™ Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current, and fast transient response. The architecture can be used in any multiphase converter ranging from 1 to 16 or more phases where flexibility facilitates the design trade-off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 2, the *XPhase*™ architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5-wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over-voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point-to-point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

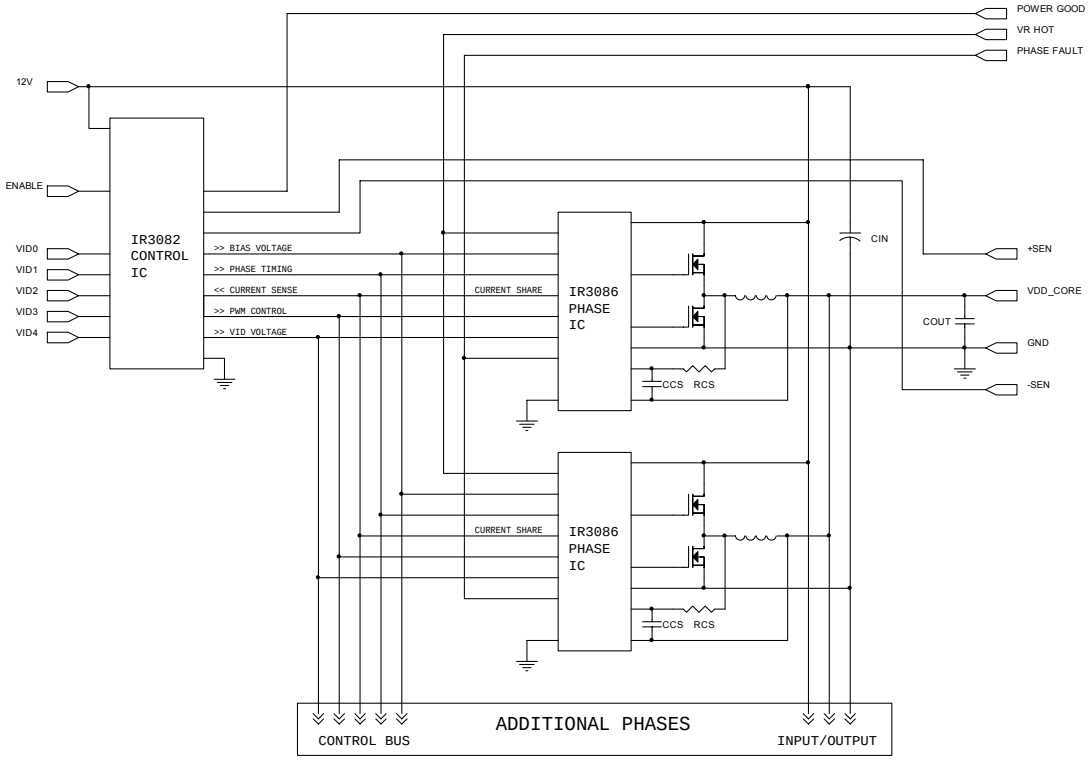


Figure 2 – System Block Diagram

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.

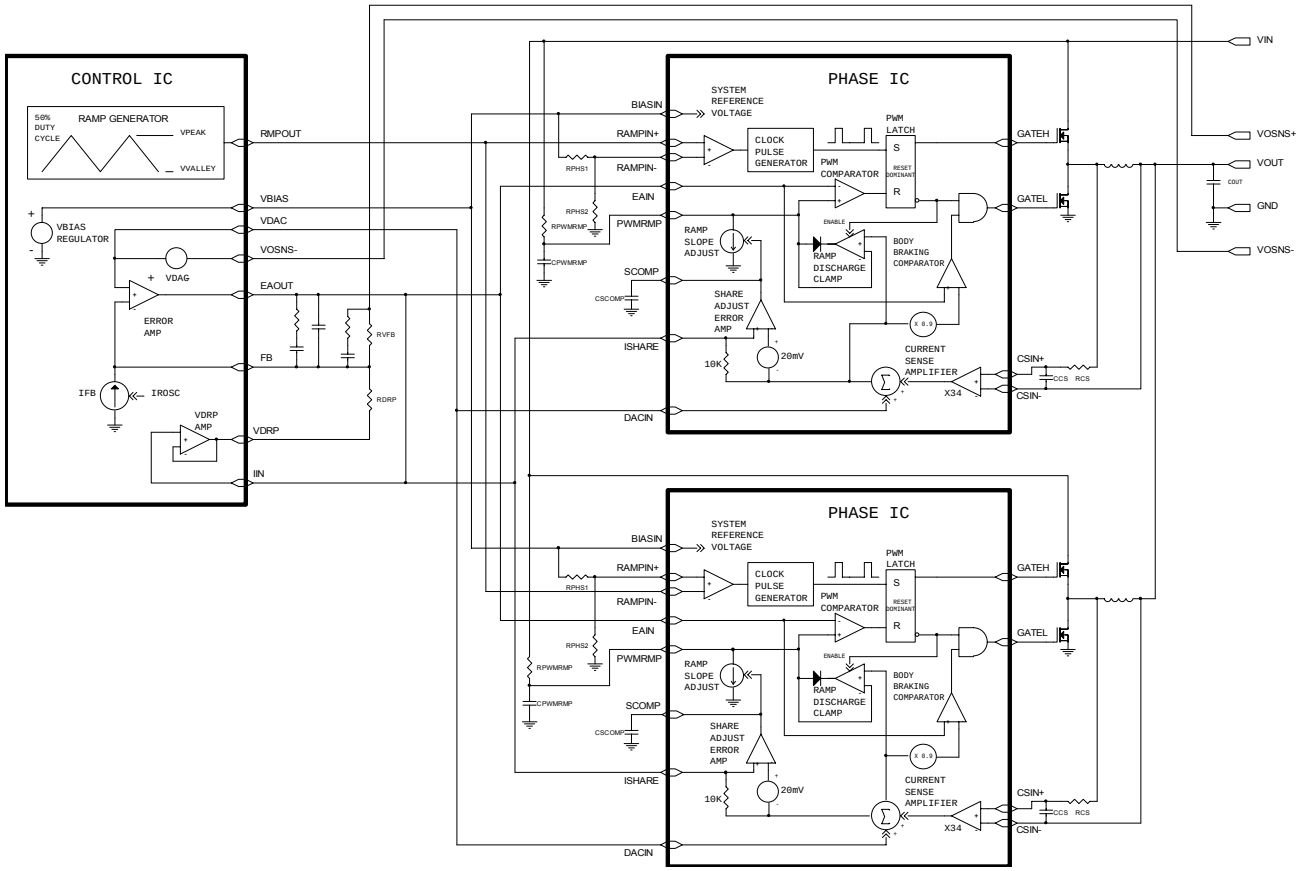


Figure 3 – IR3082 PWM Block Diagram

Frequency and Phase Timing Control

The oscillator is located in the Control IC and its frequency is programmable from 150kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 5V and 1V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 4 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP+ and RAMP- pins, as shown in Figure 3.

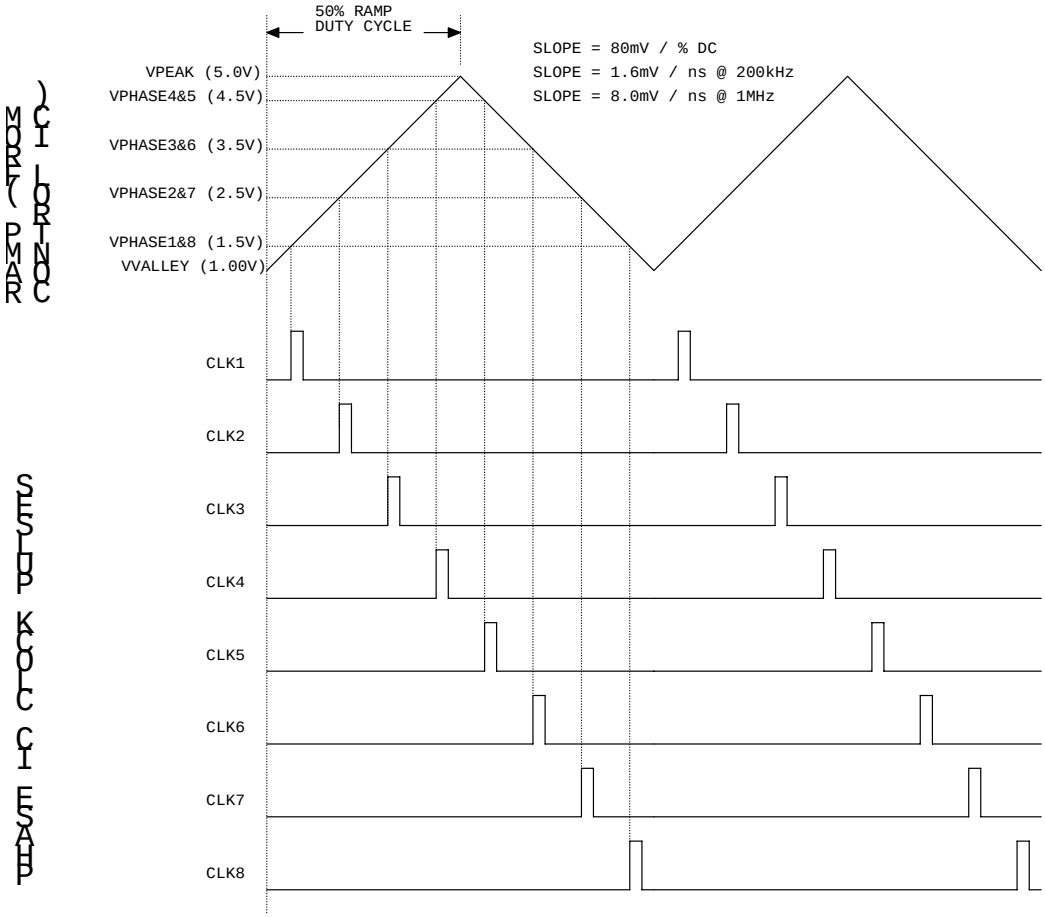


Figure 4 – 8 Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the Error Amp's output voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L \cdot (I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L \cdot (I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "Body Braking" and is accomplished through the "Body Braking Comparator" located in the Phase IC. If the Error Amp's output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

Figure 5 depicts PWM operating waveforms under various conditions.

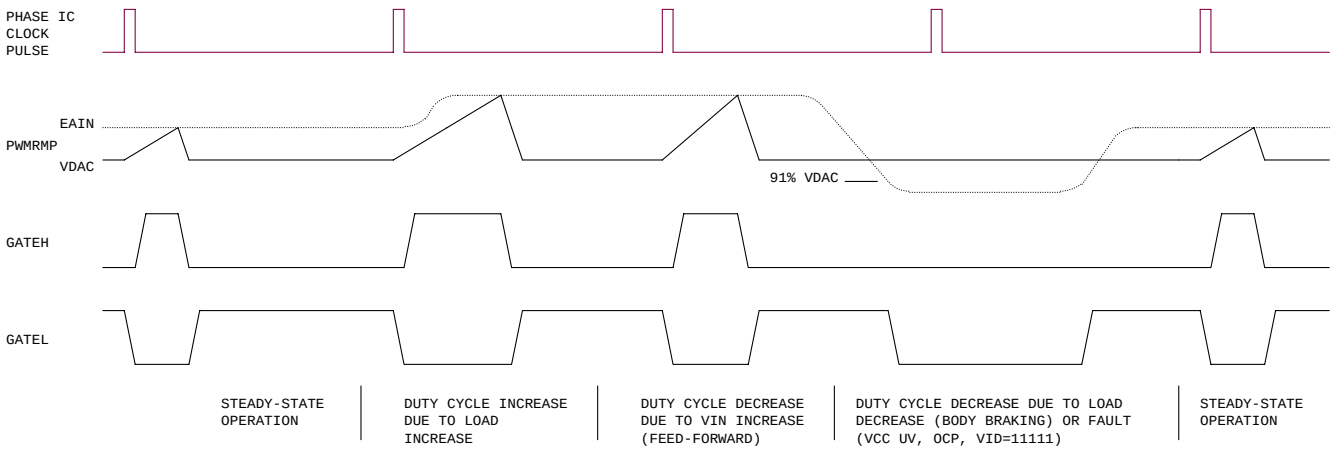


Figure 5 – PWM Operating Waveforms

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the Phase IC, as shown in figure 6. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (-1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the total current through all the inductors and is used by the Control IC for voltage positioning and current limit protection.

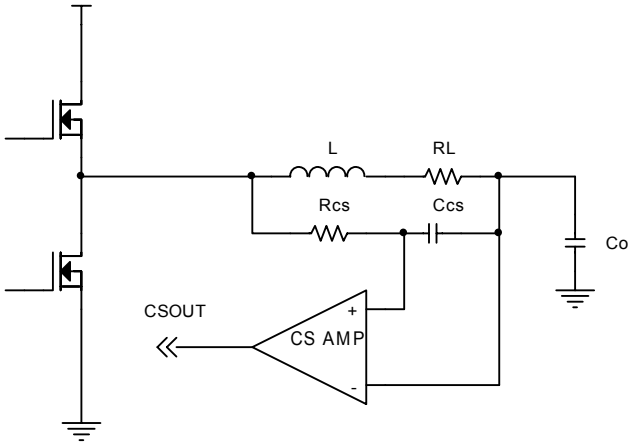


Figure 6 – Inductor Current Sensing and Current Sense Amplifier

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a 20mV offset. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

IR3082 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3082 is shown in figure 7 and discussed in the following sections.

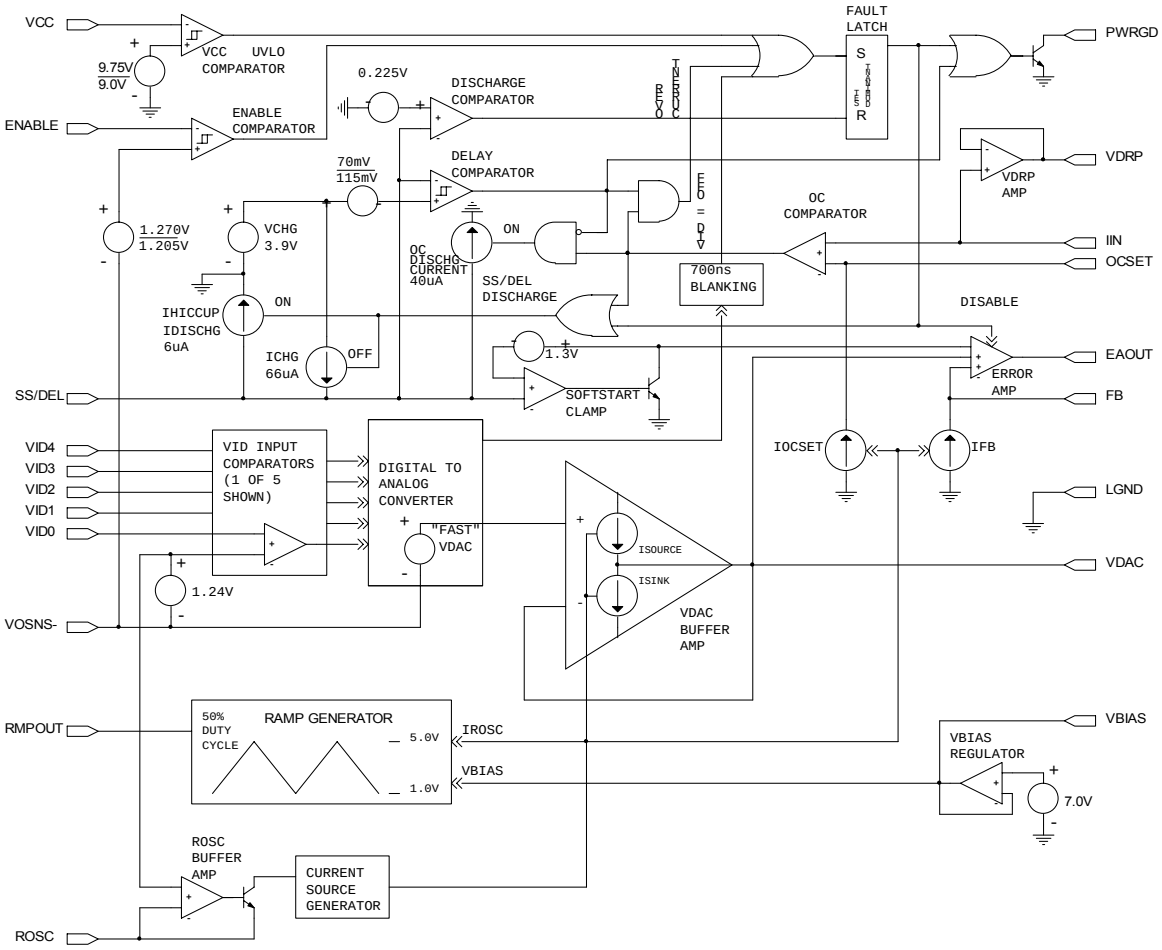


Figure 7 – IR3082 Block Diagram

VID Control

A 5-bit VID voltage compatible with AMD's Opteron/Athlon64, as shown in Table 1, is available at the VDAC pin. The VID pins require an external bias voltage and should not be floated. The VID input comparators, with 1.2V reference, monitor the VID pins and control the 6 bit Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amp is the VDAC pin. The VDAC voltage is trimmed to compensate for the input offsets of the Error Amp to provide 1% system set-point accuracy and is pre-positioned 50mV higher than Vout listed in Table1 for load positioning. The actual VDAC voltage does not determine the system accuracy and has a wider tolerance.

The IR3082 can accept changes in the VID code while operating and vary the DAC voltage accordingly. The sink/source capability of the VDAC buffer amp is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS- pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

VID4	VID3	VID2	VID1	VID0	Vout (V)
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	OFF[4]

Note: 4 Output disabled (Fault mode)

Table 1 – VID Table

Adaptive Voltage Positioning

Adaptive voltage positioning is needed to reduce the output voltage deviations during load transients and the power dissipation of the load when it is drawing maximum current. The circuitry related to voltage positioning is shown in Figure 8. Resistor R_{FB} is connected between the Error Amp's inverting input pin FB and the converter's output voltage. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency pumps current into the FB pin. The error amp forces the converter's output voltage lower to maintain a balance at its inputs. R_{FB} is selected to program the desired amount of fixed offset voltage below the DAC voltage.

The voltage at the VDRP pin is a buffered version of the share bus and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor R_{VDRP}. Since the Error Amp will force the loop to maintain FB to be equal to the VDAC reference voltage, current will flow into the FB pin equal to (VDRP-VDAC) / R_{VDRP}. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor R_{FB}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{VDRP} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

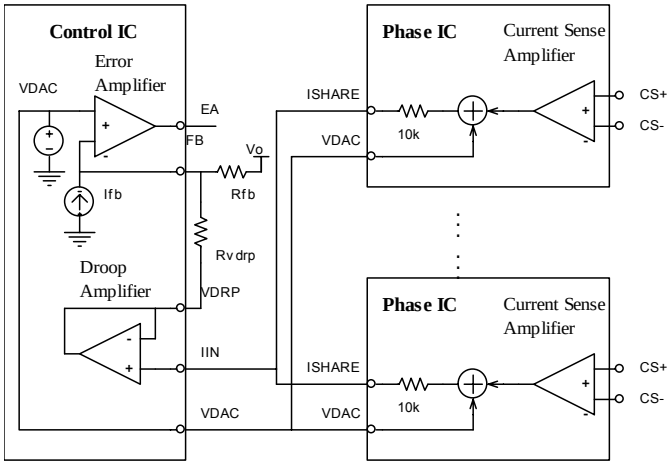


Figure 8 - Adaptive voltage positioning

Inductor DCR Temperature Correction

If the thermal compensation of the inductor DCR provided by the temperature dependent gain of the current sense amplifier is not adequate, a negative temperature coefficient (NTC) thermistor can be used for additional correction. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor as shown in Figure 9. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

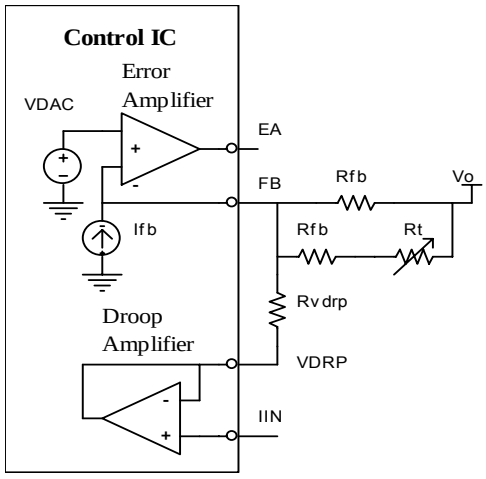


Figure 9 - Temperature compensation of inductor DCR

Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS- pin is used for remote sensing and connects directly to the load. The VDAC voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS- pins ensure that high speed transients are fed directly into the error amp without delay.

Soft Start, Over-Current Fault Delay, and Hiccup Mode

The IR3082 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start as well as over-current protection delay and hiccup mode timing. A charge current of 66uA and discharge current of 6uA control the up slope and down slope of the voltage at the SS/DEL pin respectively. Soft start-up waveforms are shown in Figure 10.

Figure 11 depicts the various operating modes as controlled by the SS/DEL function. If there is no fault, the SS/DEL pin will begin to be charged. The error amplifier output is clamped low until SS/DEL reaches 1.3V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.3V offset until it reaches the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.83V and allows the PWRGD signal to be asserted. SS/DEL finally settles at 3.9V, indicating the end of the soft start.

Under Voltage Lock Out and VID=11111 faults as well as a low signal on the ENABLE input immediately sets the fault latch causing SS/DEL to begin to discharge. The SS/DEL capacitor will continue to discharge down to 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

A delay is included if an over-current condition occurs after a successful soft start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation it will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 115mV offset of the delay comparator, the Fault latch will be set pulling the error amp's output low inhibiting switching in the phase ICs and de-asserting the PWRGD signal. The delay can be reduced by adding a resistor in series with the delay capacitor. The delay comparator's offset voltage is reduced by the drop in the resistor caused by the discharge current. To prevent the charge current from creating an offset exceeding the SS/DEL to FB input offset voltage the value of the resistor should be 10KΩ or less to avoid interference with the soft start function.

The SS/DEL capacitor will continue to discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 11 to 1 charge to discharge ratio results in a 9% hiccup mode duty cycle regardless of at what point the over-current condition occurs.

If SS/DEL pin is pulled below 0.9V, the converter can be disabled.

Under Voltage Lockout (UVLO)

The UVLO function monitors the IR3082's VCC supply pin and ensures that IR3082 has a high enough voltage to power the internal circuit. The IR3082's UVLO is set higher than the minimum operating voltage of compatible Phase ICs thus providing UVLO protection for them as well. During power-up the fault latch is reset when VCC exceeds 9.75V and there is no other fault. If the VCC voltage drops below 9.0V the fault latch will be set. For converters using a separate 5V supply for gate driver bias an external UVLO circuit can be added to prevent operation until adequate voltage is present. A diode connected between the 5V supply and the SS/DEL pin provides a simple 5V UVLO function.

Over Current Protection (OCP)

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the IIN pin voltage, which is proportional to the average current plus DAC voltage, exceeds the OCSET voltage, the over-current protection is triggered.

VID = 11111 Fault

VID code of 11111 will set the fault latch and disable the error amplifier. An 800ns delay is provided to prevent a fault condition from occurring during Dynamic VID changes.

Power Good Output

The PWRGD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PWRGD remains low until the output voltage is in regulation and SS/DEL is above 3.83V. The PWRGD pin becomes low if the fault latch is set. A high level at the PWRGD pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Load Current Indicator Output

The IIN pin voltage represents the average current of the converter plus the DAC voltage. The load current can be retrieved by subtracting the VDAC voltage from the IIN voltage.

System Reference Voltage (VBIAS)

The IR3082 supplies a 7.0V/5mA precision reference voltage from the VBIAS pin. The oscillator ramp trip points are based on the VBIAS voltage so it should be used to program the Phase ICs phase delay to minimize phase errors.

Enable Input

Pulling the ENABLE pin below 1.27V sets the Fault Latch.

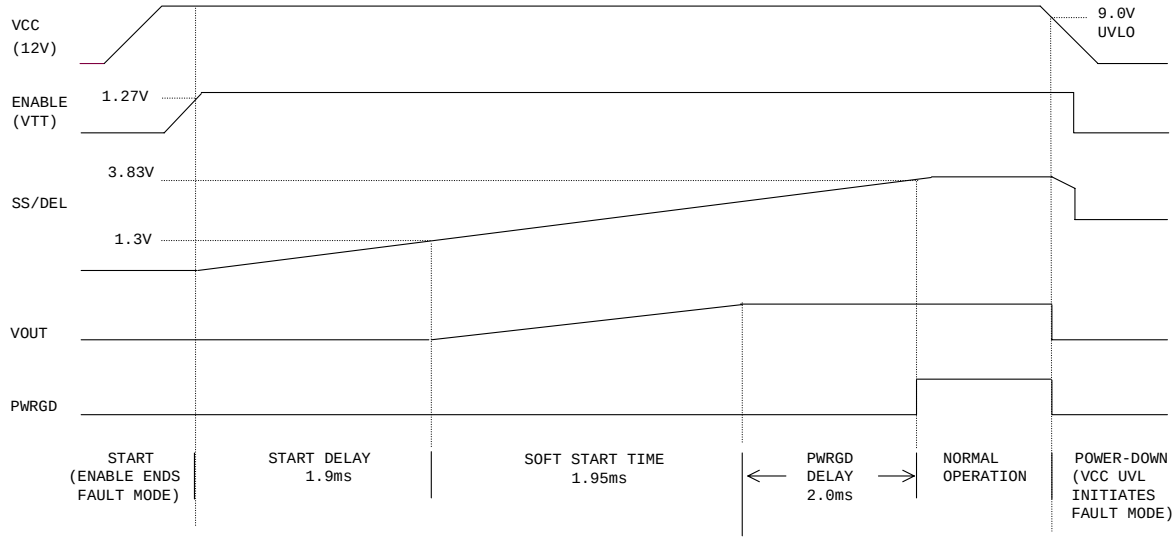


Figure 10 – Start-up Waveforms

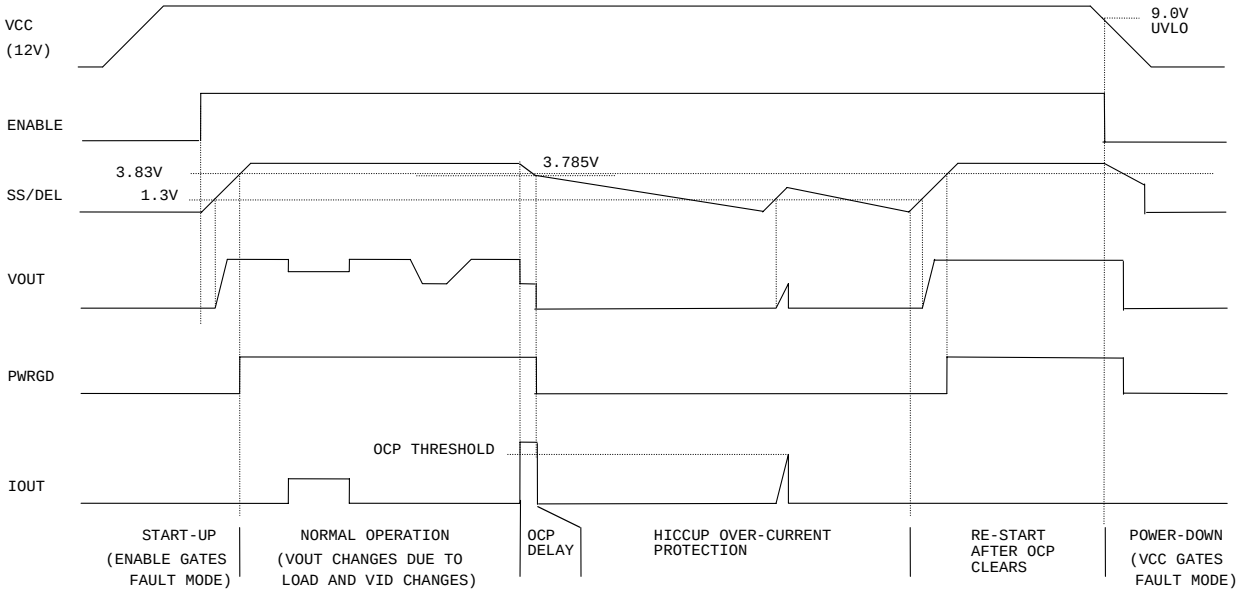


Figure 11 – Operating Waveforms

APPLICATIONS INFORMATION

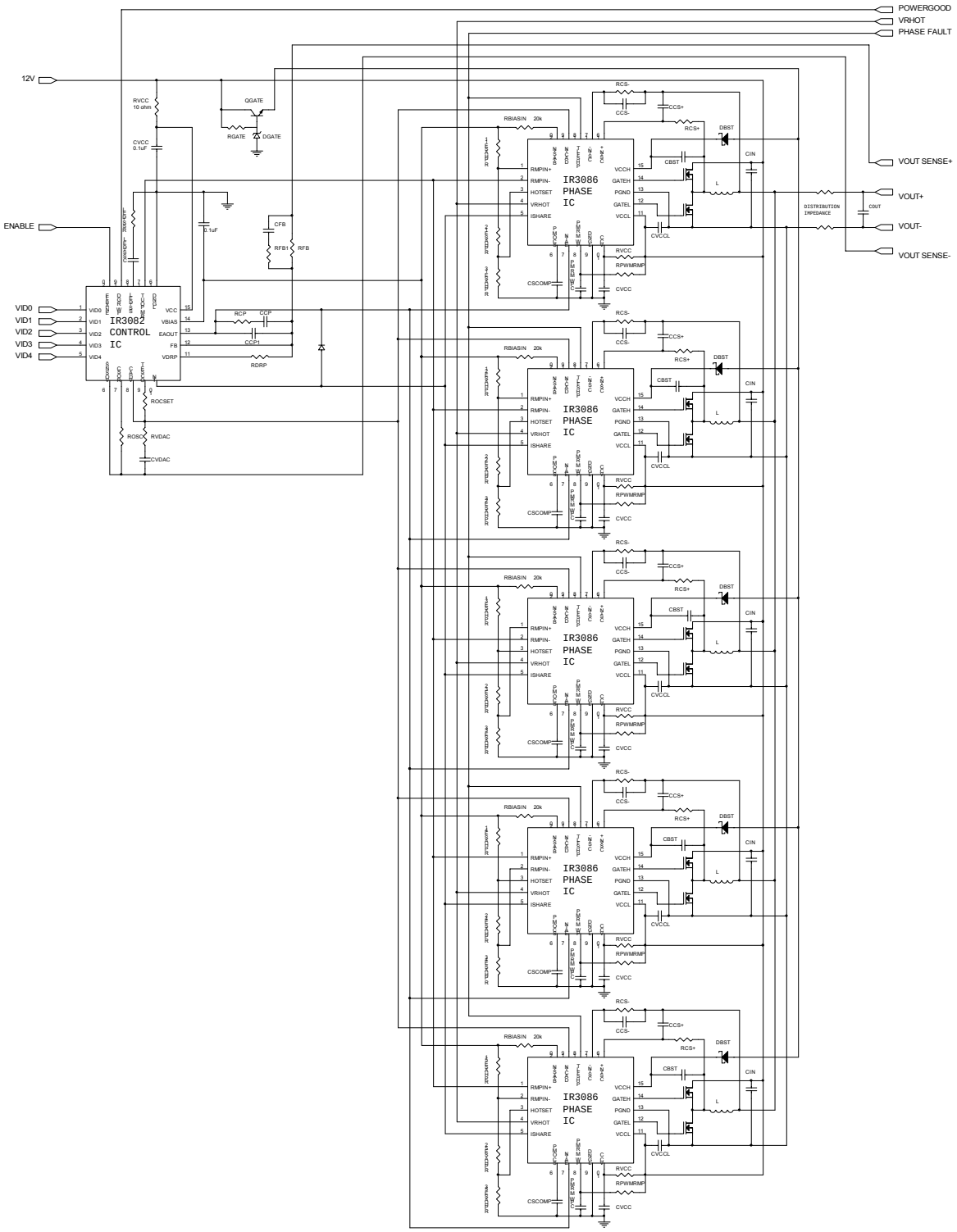


Figure 12 – IR3082/3086 5 Phase Converter for Opteron Processor

PERFORMANCE CHARACTERISTICS

Figure 13 - Oscillator Frequency vs. ROSC

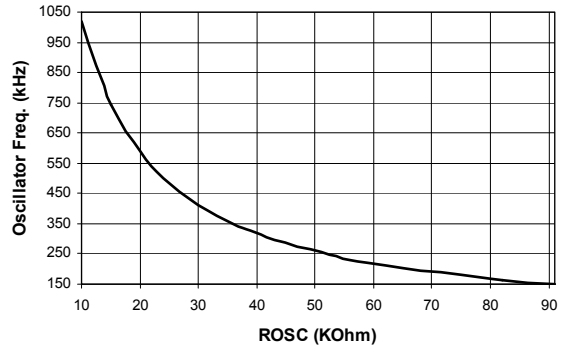


Figure 14 IFB, IOCSET vs. ROSC

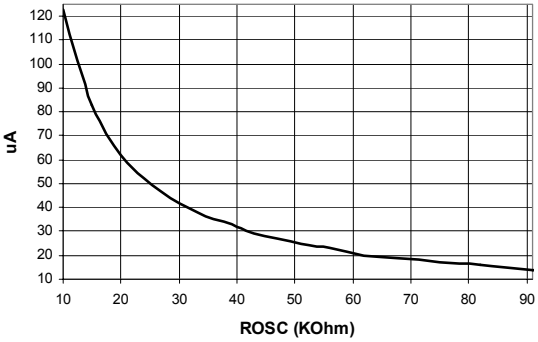


Figure 15 - VDAC Source and Sink Currents vs. ROSC

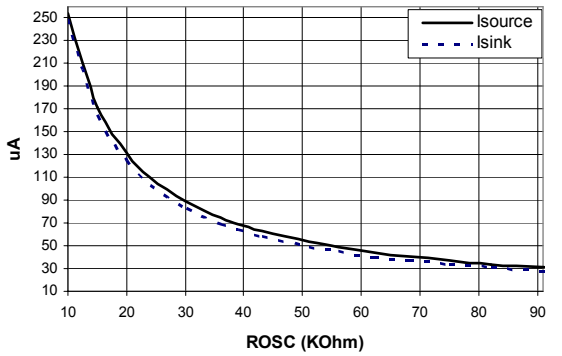


Figure 16 - Bias Current Accuracy vs. ROSC

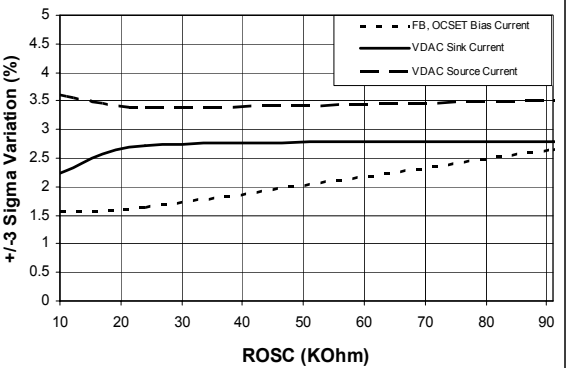
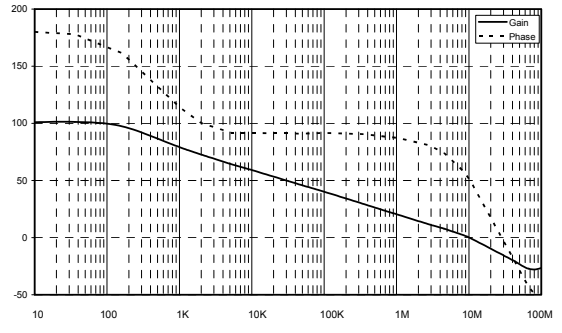


Figure 17 – Error Amplifier Frequency Response



DESIGN PROCEDURES – IR3082 AND IR3086 CHIPSET

IR3082 EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

The oscillator of IR3082 generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase converter equals the oscillator frequency, which is set by the external resistor ROSC according to the curve in Figure 13.

Soft Start Capacitor *CSS/DEL* and Resistor *RSS/DEL*

Because the capacitor CSS/DEL programs three different time parameters, i.e. soft start time, over current latch delay time, and the frequency of hiccup mode, they should be considered together while choosing CSS/DEL.

The SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10. After the ENABLE pin voltage rises above 1.23V, there is a soft-start delay time tSSDEL, after which the error amplifier output is released to allow the soft start. The soft start time tSS represents the time during which the output voltage rises from zero to Vo. tSS can be programmed by an external capacitor, which is determined by Equation (1).

$$C_{SS/DEL} = \frac{I_{CHG} \cdot t_{SS}}{V_O} = \frac{66 \cdot 10^{-6} \cdot t_{SS}}{V_O} \quad (1)$$

Once CSS/DEL is chosen, the soft start delay time tSSDEL, the over-current fault latch delay time tOCDEL, and the delay time tVccPG from output voltage (Vo) in regulation to Power Good are fixed and shown in Equations (2), (3), (4) and (5) respectively.

$$t_{SSDEL} = \frac{C_{SS/DEL} \cdot 1.3}{I_{CHG}} = \frac{C_{SS/DEL} \cdot 1.3}{66 \cdot 10^{-6}} \quad (2)$$

$$t_{OCDEL} = \frac{C_{SS/DEL} \cdot 0.09}{I_{DISCHG}} = \frac{C_{SS/DEL} \cdot 0.09}{6 \cdot 10^{-6}} \quad (3)$$

$$t_{VccPG} = \frac{C_{SS/DEL} \cdot (3.73 - V_O - 1.3)}{I_{CHG}} = \frac{C_{SS/DEL} \cdot (3.73 - V_O - 1.3)}{66 \cdot 10^{-6}} \quad (4)$$

The hiccup mode duty cycle of over current protection is determined by the charge current ICHG and discharge current IDISCHG of CSS/DEL and is fixed at 9%. However, the hiccup frequency is determined by the load current and over-current set value.

If faster over-current protection is required, a resistor in series with the soft start capacitor CSS/DEL can be used to reduce the over-current fault latch delay time tOCDEL, and the resistor RSS/DEL is determined by Equation (5). Equation (1) for soft start capacitor CSS/DEL and Equation (4) for power good delay time tVccPG are unchanged, while the equation for soft start delay time CSS/DEL (Equation 2) is changed to Equation (6).

$$R_{SSDEL} = \frac{0.09 - \frac{t_{OCDEL} \cdot I_{DISCHG}}{C_{SS/DEL}}}{I_{DISCHG}} = \frac{0.09 - \frac{t_{OCDEL} \cdot 6 \cdot 10^{-6}}{C_{SS/DEL}}}{6 \cdot 10^{-6}} \quad (5)$$

$$t_{SSDEL} = \frac{C_{SS/DEL} \cdot (1.3 - R_{SS/DEL} \cdot I_{CHG})}{I_{CHG}} = \frac{C_{SS/DEL} \cdot (1.3 - R_{SS/DEL} \cdot 66 \cdot 10^{-6})}{66 \cdot 10^{-6}} \quad (6)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope SRDOWN can be programmed by the external capacitor CVDAC as defined in Equation (7), where ISINK is the sink current of VDAC pin as shown in Figure 15. The resistor RVDAC is used to compensate VDAC circuit and is determined by Equation (8). The slew rate of VDAC up-slope SRUP is proportional to that of VDAC down-slope and is given by Equation (9), where ISOURCE is the source current of VDAC pin as shown in Figure15.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (7)$$

$$R_{VDAC} = 0.5 + \frac{3.2 \cdot 10^{-15}}{C_{VDAC}^{\ 2}} \quad (8)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} \quad (9)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 PPM, and therefore the maximum inductor DCR can be calculated from Equation (10), where RL_MAX and RL_ROOM are the inductor DCR at maximum temperature TL_MAX and room temperature T_ROOM respectively.

$$R_{L\_MAX} = R_{L\_ROOM} \cdot [1 + 3850 \cdot 10^{-6} \cdot (T_{L\_MAX} - T_{ROOM})] \quad (10)$$

The current sense amplifier gain of IR3086 decreases with temperature at the rate of 1470 PPM, which compensates part of the inductor DCR increase. The phase IC die temperature is only a couple of degrees Celsius higher than the PCB temperature due to the low thermal impedance of MLPQ package. The minimum current sense amplifier gain at the maximum phase IC temperature TIC_MAX is calculated from Equation (11).

$$G_{CS\_MIN} = G_{CS\_ROOM} \cdot [1 - 1470 \cdot 10^{-6} \cdot (T_{IC\_MAX} - T_{ROOM})] \quad (11)$$

The total input offset voltage (VCS_TOFST) of current sense amplifier in phase ICs is the sum of input offset (VCS_OFST) of the amplifier itself and that created by the amplifier input bias currents flowing through the current sense resistors RCS+ and RCS-.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} \cdot R_{CS+} - I_{CSIN-} \cdot R_{CS-} \quad (12)$$

The over current limit is set by the external resistor ROCSET as defined in Equation (13), where ILIMIT is the required over current limit. IOCSET, the bias current of OCSET pin, changes with switching frequency setting resistor ROSC and is determined by the curve in Figure 14. KP is the ratio of inductor peak current over average current in each phase and is calculated from Equation (14).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} \cdot R_{L\_MAX} \cdot (1 + K_P) + V_{CS\_TOFST}] \cdot G_{CS\_MIN} / I_{OCSET} \quad (13)$$

$$K_P = \frac{(V_I - V_O) \cdot V_O / (L \cdot V_I \cdot f_{SW} \cdot 2)}{I_O / n} \quad (14)$$

No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP*

A resistor between FB pin and the converter output is used to create output voltage offset V_{O_NLOFST}, which is the difference between V_{DAC} voltage and output voltage at no load condition. Adaptive voltage positioning lowers the converter voltage by Ro times Io, where Ro is the required output impedance of the converter.

R_{FB} is not only determined by I_{FB}, the current flowing out of the FB pin as shown in Figure 14, but also affected by the total input offset voltage of current sense amplifiers. R_{FB} and R_{DRP} are determined by (15) and (16) respectively.

$$R_{FB} = \frac{R_{L\_MAX} \cdot V_{O\_NLOFST} - V_{CS\_TOFST} \cdot n \cdot R_O}{I_{FB} \cdot R_{L\_MAX}} \quad (15)$$

$$R_{DRP} = \frac{R_{FB} \cdot R_{L\_MAX} \cdot G_{CS\_MIN}}{n \cdot R_O} \quad (16)$$

IR3086 EXTERNAL COMPONENTS

PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP*

PWM ramp is generated by connecting the resistor R_{PWMRMP} between a voltage source and PWMRMP pin as well as the capacitor C_{PWMRMP} between PWMRMP and LGND. Choose the desired PWM ramp magnitude V_{RAMP} and the capacitor C_{PWMRMP} in the range of 100pF and 470pF, and then calculate the resistor R_{PWMRMP} from Equation (17). To achieve feed-forward voltage mode control, the resistor R_{RAMP} should be connected to the input of the converter.

$$R_{PWMRMP} = \frac{V_O}{V_{IN} \cdot f_{SW} \cdot C_{PWMRMP} \cdot [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]} \quad (17)$$

Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor R_{CS+} and capacitor C_{CS+} in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor C_{CS+} represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance R_L. Pre-select the capacitor C_{CS+} and calculate R_{CS+} as follows.

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} \quad (18)$$

The bias current flowing out of the non-inverting input of the current sense amplifier creates a voltage drop across R_{CS+}, which is equivalent to an input offset voltage of the current sense amplifier. The offset affects the accuracy of converter current signal ISHARE as well as the accuracy of the converter output voltage if adaptive voltage positioning is adopted. To reduce the offset voltage, a resistor R_{CS-} should be added between the amplifier inverting input and the converter output. The resistor R_{CS-} is determined by the ratio of the bias current from the non-inverting input and the bias current from the inverting input.

$$R_{CS-} = \frac{I_{CSIN+}}{I_{CSIN-}} \cdot R_{CS+} \quad (19)$$

If R_{CS-} is not used, R_{CS+} should be chosen so that the offset voltage is small enough. Usually R_{CS+} should be less than 2 kΩ and therefore a larger C_{CS+} value is needed.

Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is proportional to the die temperature T_J (ºC) of phase IC. Determine the relationship between the die temperature of phase IC and the temperature of the power converter according to the power loss, PCB layout and airflow etc, and then calculate HOTSET threshold voltage corresponding to the allowed maximum temperature from Equation (20).

$$V_{HOTSET} = 4.73 \cdot 10^{-3} \cdot T_J + 1.241 \quad (20)$$

There are two ways to set the over temperature threshold, central setting and local setting. In the central setting, only one resistor divider is used, and the setting voltage is connected to HOTSET pins of all the phase ICs. To reduce the influence of noise on the accuracy of over temperature setting, a 0.1uF capacitor should be placed next to HOTSET pin of each phase IC. In the local setting, a resistor divider per phase is needed, and the setting voltage is connected to HOTSET pin of each phase. The 0.1uF decoupling capacitor is not necessary. Use VBIAS as the reference voltage. If $R_{HOTSET1}$ is pre-selected, $R_{HOTSET2}$ can be calculated as follows.

$$R_{HOTSET2} = \frac{R_{HOTSET1} \cdot V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} \quad (21)$$

Phase Delay Timing Resistors *RPHASE1* and *RPHASE2*

The phase delay of the interleaved multiphase converter is programmed by the resistor divider connected at RMPIN+ or RMPIN- depending on which slope of the oscillator ramp is used for the phase delay programming of phase IC, as shown in Figure 3.

If the upslope is used, RMPIN+ pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN- pin should be connected to the resistor divider. When RMPOUT voltage is above the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

If down slope is used, RMPIN- pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN+ pin should be connected to the resistor divider. When RMPOUT voltage is below the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

Use VBIAS voltage as the reference for the resistor divider since the oscillator ramp magnitude from control IC tracks VBIAS voltage. Try to avoid both edges of the oscillator ramp for better noise immunity. Determine the ratio of the programming resistors, RA_{PHASEx}, corresponding to the desired switching frequencies and phase numbers. If the resistor $R_{PHASEx1}$ is pre-selected, the resistor $R_{PHASEx2}$ is determined as:

$$R_{PHASEx2} = \frac{RA_{PHASEx} \cdot R_{PHASEx1}}{1 - RA_{PHASEx}} \quad (22)$$

Combined Over Temperature and Phase Delay Setting Resistors *RPHASE1*, *RPHASE2* and *RPHASE3*

The over temperature setting resistor divider can be combined with the phase delay resistor divider to save one resistor per phase.

Calculate the HOTSET threshold voltage V_{HOTSET} corresponding to the allowed maximum temperature from Equation (20). If the over temperature setting voltage is lower than the phase delay setting voltage, VBIAS*RA_{PHASEx}, connect RMPIN+ or RMPIN- pin between $R_{PHASEx1}$ and $R_{PHASEx2}$ and connect HOTSET pin between $R_{PHASEx2}$ and $R_{PHASEx3}$ respectively. Pre-select $R_{PHASEx1}$, then calculate $R_{PHASEx2}$ and $R_{PHASEx3}$,

$$R_{PHASEx2} = \frac{(RA_{PHASEx} \cdot V_{BIAS} - V_{HOTSET}) \cdot R_{PHASEx1}}{V_{BIAS} \cdot (1 - RA_{PHASEx})} \quad (23)$$

$$R_{PHASEx3} = \frac{V_{HOTSET} \cdot R_{PHASEx1}}{V_{BIAS} \cdot (1 - RA_{PHASEx})} \quad (24)$$

If the over temperature setting voltage is higher than the phase delay setting voltage, VBIAS times RA_{PHASEx}, connect HOTSET pin between $R_{PHASEx1}$ and $R_{PHASEx2}$ and connect RMPIN+ or RMPIN- between $R_{PHASEx2}$ and $R_{PHASEx3}$ respectively. Pre-select $R_{PHASEx1}$,

$$R_{PHASEx2} = \frac{(V_{HOTSET} - RA_{PHASEx} \cdot V_{BIAS}) \cdot R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (25)$$

$$R_{PHASEx3} = \frac{RA_{PHASEx} \cdot V_{BIAS} \cdot R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (26)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a 0.1uF to 1uF capacitor is needed for the bootstrap circuit.

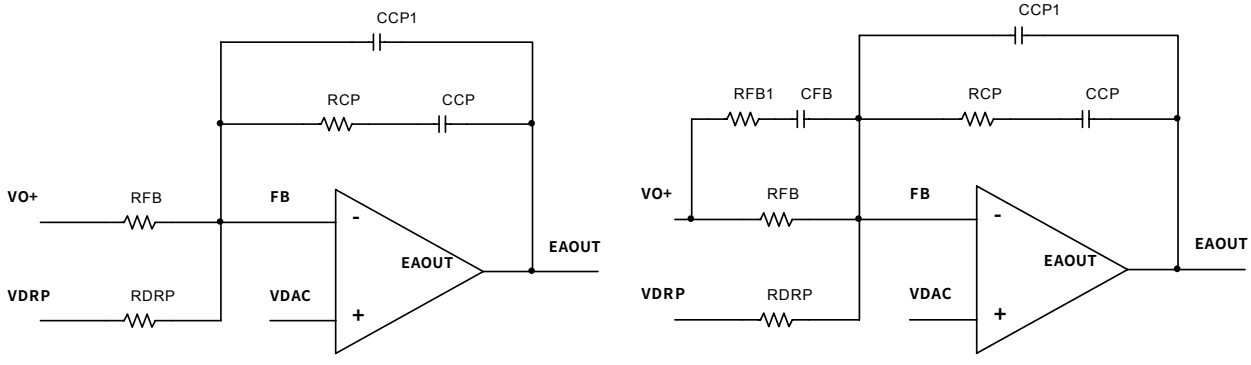
Decoupling Capacitors for Phase IC

0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

VOLTAGE LOOP COMPENSATION

The adaptive voltage positioning (AVP is usually used in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Resistors R_{FB} and R_{DRP} are chosen according to Equations (15) and (16), and the selection of compensation types depends on the capacitors used. For the applications using Electrolytic, Polymer or AL-Polymer capacitors, type II compensation shown in Figure 18 (a) is usually enough. While for the applications with only ceramic capacitors, type III compensation shown in Figure 18 (b) is preferred.



(a) Type II compensation (b) Type III compensation

Figure 18. Voltage loop compensation network

Type II Compensation

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, R_{CP} and C_{CP} can be determined by equations (27) and (28).

$$R_{CP} = \frac{(2\pi \cdot f_C)^2 \cdot L_E \cdot C_E \cdot R_{FB} \cdot V_{PWMRMP}}{\sqrt{1+(2\pi \cdot f_C \cdot C_E \cdot R_{CE})^2} \cdot V_o} \quad (27)$$

$$C_{CP} = \frac{10 \cdot \sqrt{L_E \cdot C_E}}{R_{CP}} \quad (28)$$

where L_E and R_{CE} are the equivalent output inductance and ESR of output capacitors respectively. C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, R_{CP} and C_{CP} can be determined by equations (29) and (30), where C_E is equivalent output capacitance.

$$R_{CP} = \frac{(2\pi \cdot f_C)^2 \cdot L_E \cdot C_E \cdot V_{PWMRMP}}{V_o} \quad (29)$$

$$C_{CP} = \frac{10 \cdot \sqrt{L_E \cdot C_E}}{R_{CP}} \quad (30)$$

Choose resistor R_{FB1} according to Equation (31), and determine C_{FB} from Equations (32).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (31)$$

$$C_{FB} = \frac{1}{4\pi \cdot f_{C1} \cdot R_{FB1}} \quad (32)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop should be at least one decade lower than that of the voltage loop in order to eliminate the interaction between the two loops. A capacitor from SCOMP to LGND is usually enough for most of the applications. Choose the crossover frequency of current share loop (f_{CI}) based on the crossover frequency of voltage loop (f_C), and determine the C_{SCOMP},

$$C_{SCOMP} = \frac{0.65 \cdot R_{PWMRMP} \cdot V_I \cdot I_O \cdot G_{CS\_ROOM} \cdot R_{LE} \cdot [1+2\pi \cdot f_{CI} \cdot C_E \cdot (V_O/I_O)] \cdot F_{MI}}{V_O \cdot 2\pi \cdot f_{CI} \cdot 1.05 \cdot 10^6} \quad (33)$$

Where FMI is the PWM gain in the current share loop,

$$C_{SCOMP} = \frac{R_{PWMRMP} \cdot C_{PWMRMP} \cdot f_{SW} \cdot V_{PWMRMP}}{(V_O - V_{PWMRMP} - V_{DAC}) \cdot (V_I - V_{DAC})} \quad (34)$$

DESIGN EXAMPLE — 5-PHASE OPTERON CONVERTER

SPECIFICATIONS

Input Voltage: V_I=12 V
DAC Voltage: V_{DAC}=1.3 V
No Load Output Voltage Offset: V_{O_NLOFST}=15mV
Maximum Output Current: I_{OMAX}=100 ADC
Output Impedance: R_O=0.75 mΩ
Soft Start Time: t_{SS} = 2 mS
Dynamic VID Down-Slope Slew Rate: SR_{DOWN}=2.5mV/uS
Over Temperature Threshold: T_{PCB}=115 ºC

POWER STAGE

Phase Number: n=5
Switching Frequency: f_{SW}=600 kHz
Output Inductors: L=220 nH, R_L=0.42 mΩ
Output Capacitors: C=47uF, R_C= 2mΩ, Number Cn=32

IR3082 EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, R_{OSC} can be determined from the curve in Figure 13. For switching frequency of 600kHz per phase, choose R_{OSC}=18.2kΩ

Soft Start Capacitor *CSS/DEL*

Calculate the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{I_{CHG} \cdot t_{SS}}{V_O} = \frac{66 \cdot 10^{-6} \cdot 2 \cdot 10^{-3}}{1.3 + (50-15) \cdot 10^{-3}} = 0.0988uF$$, choose $C_{SS/DEL} = 0.1uF$

The soft start delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} \cdot 0.09}{I_{DISCHG}} = \frac{C_{SS/DEL} \cdot 0.09}{6 \cdot 10^{-6}} = 1.5ms$$

$$t_{VccPG} = \frac{C_{SS/DEL} \cdot (3.73 - V_O - 1.3)}{I_{CHG}} = \frac{0.1 \cdot 10^{-6} \cdot (3.73 - 1.335 - 1.3)}{66 \cdot 10^{-6}} = 1.64ms$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

From Figure 15, the sink current of VDAC pin corresponding to 600kHz (R_{OSC}=18.2kΩ) is 125uA. Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{125 \cdot 10^{-6}}{2.5 \cdot 10^{-3} / 10^{-6}} = 50nF$$, Choose C_{VDAC}=47nF

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2 \cdot 10^{-15}}{C_{VDAC}^{\ 2}} = 0.5 + \frac{3.2 \cdot 10^{-15}}{(47 \cdot 10^{-9})^2} = 2\Omega$$

From Figure 15, the source current of VDAC pin is 170uA. The VDAC up-slope slew rate is

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{170 \cdot 10^{-6}}{47 \cdot 10^{-9}} = 3.6mV / uS$$

Over Current Setting Resistor *ROCSET*

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} \cdot [1 + 3850 \cdot 10^{-6} \cdot (T_{L\_MAX} - T_{ROOM})] = 0.42 \cdot 10^{-3} \cdot [1 + 3850 \cdot 10^{-6} \cdot (100 - 25)] = 0.54m\Omega$$

The current sense amplifier gain is 34 at 25ºC, and its gain at 101ºC is calculated as,

$$G_{CS\_MIN} = G_{CS\_ROOM} \cdot [1 - 1470 \cdot 10^{-6} \cdot (T_{IC\_MAX} - T_{ROOM})] = 34 \cdot [1 - 1470 \cdot 10^{-6} \cdot (101 - 25)] = 30.2$$

Set the over current limit at 115A. From Figure 14, the bias current of OCSET pin (I_{OCSET}) is 65uA with R_{OSC}=18.2kΩ. The total current sense amplifier input offset voltage is 0.6mV, which includes the offset created by the current sense amplifier input resistor mismatch.

Calculate constant K_P, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{(V_I - V_O) \cdot V_O / (L \cdot V_I \cdot f_{SW} \cdot 2)}{I_{LIMIT} / n} = \frac{(12 - 1.335) \cdot 1.335 / (220 \cdot 10^{-9} \cdot 12 \cdot 600 \cdot 10^3 \cdot 2)}{115 / 5} = 0.147$$

$$R_{OCSET} = [\frac{R_{LIMIT}}{n} \cdot R_{L\_MAX} \cdot (1 + K_P) + V_{CS\_TOFST}] \cdot G_{CS\_MIN} / I_{OCSET}$$

$$= (\frac{115}{5} \cdot 0.54 \cdot 10^{-3} \cdot 1.147 + 0.6 \cdot 10^{-3}) \cdot 30.2 / (65 \cdot 10^{-6}) = 6.9k\Omega$$

No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP*

From Figure 14, the bias current of FB pin is 65uA with R_{OSC}=18.2kΩ.

$$R_{FB} = \frac{R_{L\_MAX} \cdot V_{O\_NLOFST} - V_{CS\_TOFST} \cdot n \cdot R_O}{I_{FB} \cdot R_{L\_MAX}} = \frac{0.54 \cdot 10^{-3} \cdot 15 \cdot 10^{-3} - 0.6 \cdot 10^{-3} \cdot 5 \cdot 0.75 \cdot 10^{-3}}{65 \cdot 10^{-6} \cdot 0.54 \cdot 10^{-3}} = 230\Omega$$

Select RFB = 232 Ω.

$$R_{DRP} = \frac{R_{FB} \cdot R_{L\_MAX} \cdot G_{CS\_MIN}}{n \cdot R_O} = \frac{232 \cdot 0.54 \cdot 10^{-3} \cdot 30.2}{5 \cdot 0.75 \cdot 10^{-3}} = 1.01k\Omega$$

IR3086 EXTERNAL COMPONENTS

PWM Ramp Resistor *RRAMP* and Capacitor C*RAMP*

Set PWM ramp magnitude V_{PWMRMP}=0.8V. Choose 100pF for PWM ramp capacitor C_{PWMRMP}, and calculate the resistor R_{PWMRMP},

$$R_{PWMRMP} = \frac{V_O}{V_{IN} \cdot f_{SW} \cdot C_{PWMRMP} \cdot [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]}$$

$$= \frac{1.30}{12 \cdot 600 \cdot 10^3 \cdot 100 \cdot 10^{-12} \cdot [\ln(12 - 1.30) - \ln(12 - 1.30 - 0.8)]} = 17.9k\Omega$$, choose R_{PWMRMP}=18.2kΩ

Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

Choose C_{CS+}=47nF and calculate R_{CS+},

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{220 \cdot 10^{-9} / (0.42 \cdot 10^{-3})}{47 \cdot 10^{-9}} = 11.2k\Omega$$

Choose $R_{CS+} = 11.5k\Omega$. The bias currents of CSIN+ and CSIN- are 0.25uA and 0.4uA respectively. Calculate resistor R_{CS-},

$$R_{CS-} = \frac{0.25}{0.4} \cdot R_{CS+} = \frac{0.25}{0.4} \cdot 10.0 \cdot 10^3 = 7.19k\Omega$$, choose R_{CS-}=7.15kΩ

Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

Use central over temperature setting and set the temperature threshold at 115 ºC, which corresponds the IC die temperature of 116 ºC. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

$$V_{HOTSET} = 4.73 \cdot 10^{-3} \cdot T_J + 1.241 = 4.73 \cdot 10^{-3} \cdot 116 + 1.241 = 1.79V$$, choose $R_{HOTSET1}$=20.0kΩ,

$$R_{HOTSET2} = \frac{R_{HOTSET1} \cdot V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} = \frac{20 \cdot 10^3 \cdot 1.79}{6.8 - 1.79} = 7.14k\Omega$$

Phase Delay Timing Resistors *RPHASE1* and *RPHASE2*

The phase delay resistor ratios for phases 1 to 5 at 600kHz of switching frequencies are RAPHASE1=0.646, RAPHASE2=0.400, RAPHASE3=0.158, RAPHASE4=0.291 and RAPHASE5=0.561 starting from down-slope. Pre-select RPHASE11=RPHASE21=RPHASE31=RPHASE41=RPHASE51= RPHASE61=20kΩ,

$$R_{PHASE12} = \frac{RA_{PHASE1}}{1 - RA_{PHASE1}} \cdot R_{PHASE11} = \frac{0.646}{1 - 0.646} \cdot 20 \cdot 10^3 = 36.5k\Omega$$

$R_{PHASE22}$=13.3kΩ, $R_{PHASE32}$=3.74kΩ, $R_{PHASE42}$=8.2kΩ, $P_{PHASE52}$=25.5kΩ

Bootstrap Capacitor C$_{BST}$

Choose C_{BST}=0.1uF

Decoupling Capacitors for Phase IC and Power Stage

Choose C_{VCC}=0.1uF, C_{VCCL}=0.1uF

VOLTAGE LOOP COMPENSATION

All ceramic output capacitors are used in the design, type III compensation as shown in Figure 18(b) is used here. Choose the desired crossover frequency fc =80 kHz and determine Rcp and C_{CP}:

$$R_{CP} = \frac{(2\pi \cdot f_C)^2 \cdot L_E \cdot C_E \cdot R_{FB} \cdot V_{PWMRMP}}{V_o} = \frac{(2\pi \cdot 80 \cdot 10^3)^2 \cdot (220 \cdot 10^{-9}/5) \cdot (47 \cdot 10^{-6} \cdot 32) \cdot 230 \cdot 0.8}{1.335} = 2.31k\Omega$$

$$C_{CP} = \frac{10 \cdot \sqrt{L_E \cdot C_E}}{R_{CP}} = \frac{10 \cdot \sqrt{(220 \cdot 10^{-9}/5) \cdot (47 \cdot 10^{-6} \cdot 32)}}{2.31 \cdot 10^3} = 35.2nF$$, Choose C_{CP}=33nF

$$R_{FB1} = \frac{1}{2} \cdot R_{FB} = \frac{1}{2} \cdot 230 = 115\Omega$$ Choose R_{FB1}=100Ω

$$C_{FB} = \frac{1}{4\pi \cdot f_C \cdot R_{FB1}} = \frac{1}{4\pi \cdot 80 \cdot 10^3 \cdot 100} = 8.54nF$$, choose C_{FB}=10nF

Choose C_{CP1}=220pF to reduce high frequency noise.

CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop f_{CI} should be at least one decade lower than that of the voltage loop f_C. Choose the crossover frequency of current share loop f_{CI}=10kHz, and calculate C_{SCOMP},

$$F_{MI} = \frac{R_{PWMRMP} \cdot C_{PWMRMP} \cdot f_{SW} \cdot V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) \cdot (V_I - V_{DAC})} = \frac{18.2 \cdot 10^3 \cdot 100 \cdot 10^{-12} \cdot 600 \cdot 10^3 \cdot 0.8}{(12 - 0.8 - 1.35) \cdot (12 - 1.35)} = 0.011$$

$$C_{SCOMP} = \frac{0.65 \cdot R_{PWMRMP} \cdot V_I \cdot I_O \cdot G_{CS\_ROOM} \cdot R_{LE} \cdot [1 + 2\pi \cdot f_{CI} \cdot C_E \cdot (V_O / I_O)] \cdot F_{MI}}{V_O \cdot 2\pi \cdot f_{CI} \cdot 1.05 \cdot 10^6}$$

$$= \frac{0.65 \cdot 18.2 \cdot 10^3 \cdot 12 \cdot 100 \cdot 34 \cdot (0.42 \cdot 10^{-3}/5) \cdot [1 + 2\pi \cdot 10 \cdot 10^3 \cdot 1504 \cdot 10^{-6} \cdot (1.33 - 100 \cdot 7.5 \cdot 10^{-4})/100] \cdot 0.011}{(1.33 - 100 \cdot 7.5 \cdot 10^{-4}) \cdot 2\pi \cdot 10 \cdot 10^3 \cdot 1.05 \cdot 10^6}$$

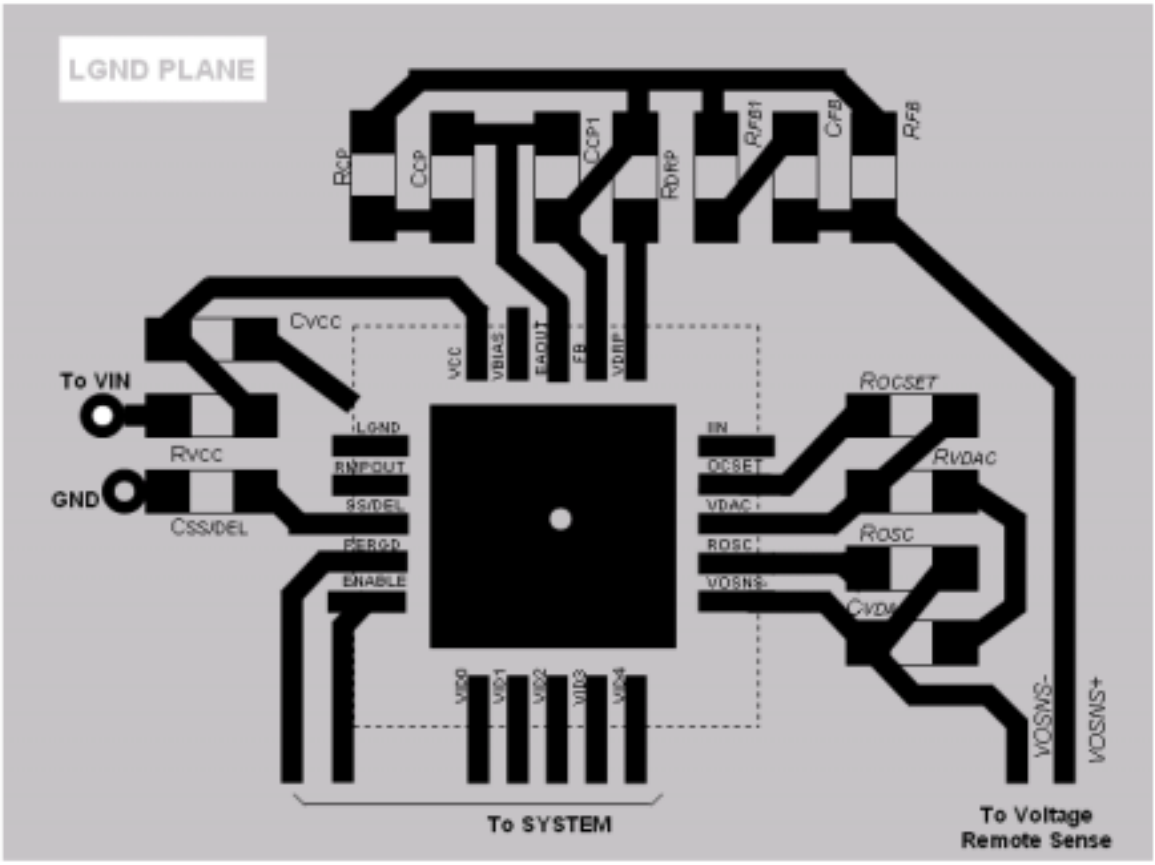
$$= 12.4nF$$

Choose C_{SCOMP}=22nF

LAYOUT GUIDELINES

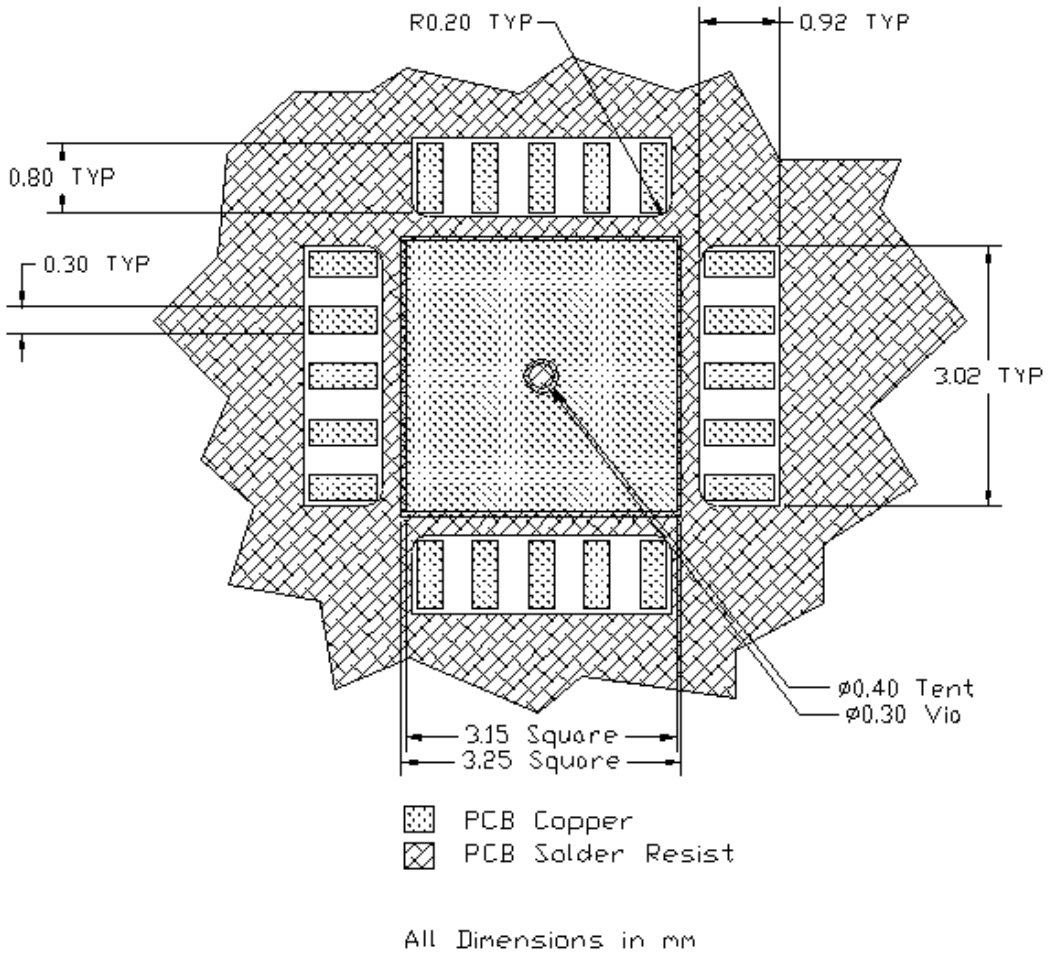
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, CVCC, CSS/DEL and RCC/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Control bus signals, VDAC, RMPOUT, IIN, VBIAS, and especially EAOUT, should not cross over the fast transition nodes.



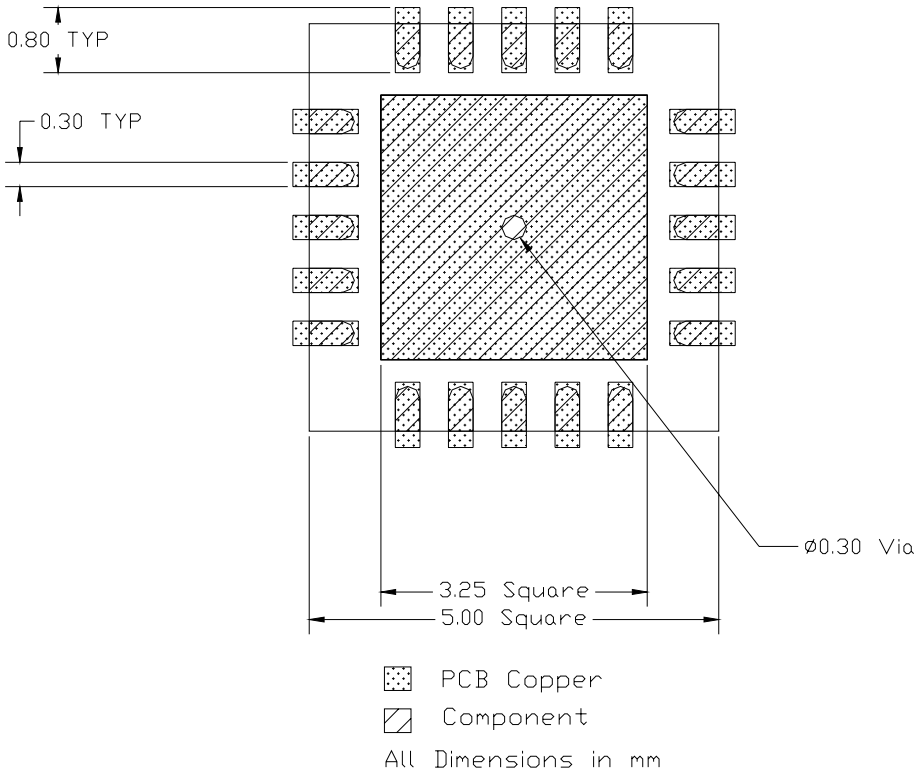
METAL AND SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm, therefore it is recommended that the solder resist is completely removed from between the lead lands forming a single opening for each "group" of lead lands.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The single via in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



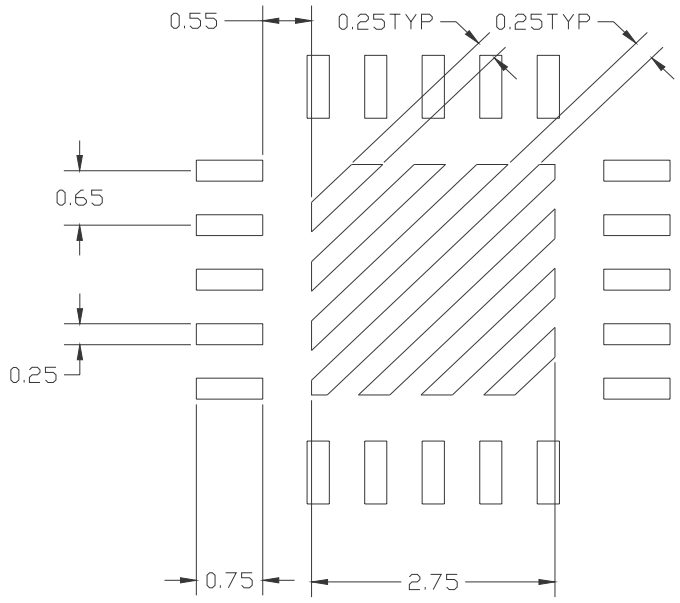
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.2 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



STENCIL DESIGN

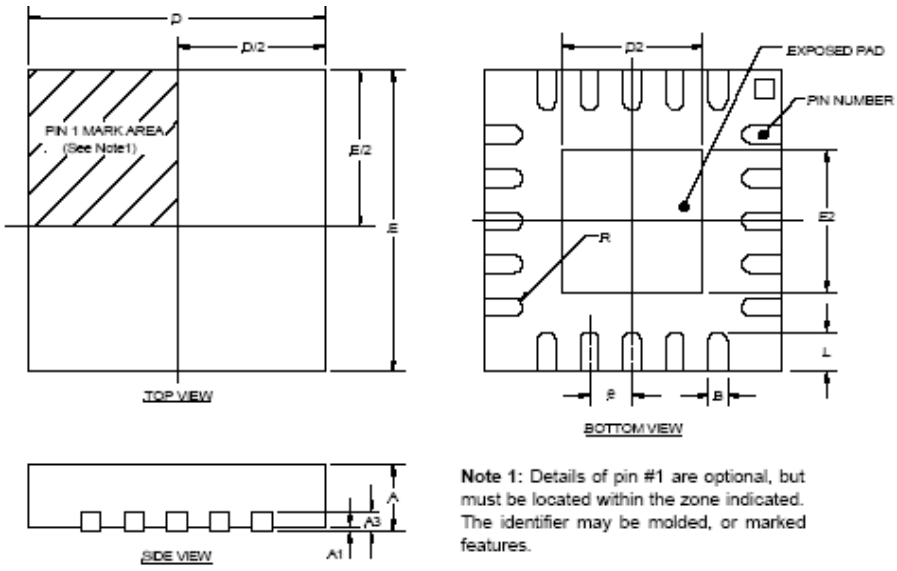
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

20L MLPQ (5 x 5 mm Body) – θ_{JA} = 30°C/W, θ_{JC} = 3°C/W



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	20-PIN 5x5		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.23	0.30	0.38
D		5.00 BSC	
D2	3.00	3.15	3.25
E		5.00 BSC	
E2	3.00	3.15	3.25
e		0.65 BSC	
L	0.45	0.55	0.65
R	0.115	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

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