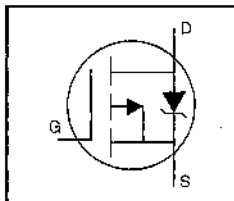


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DS} = -200V$$

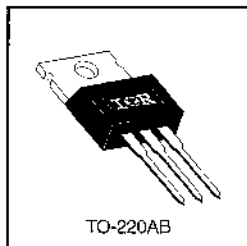
$$R_{DS(on)} = 0.50\Omega$$

$$I_D = -11A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

 DATA
SHEETS

Absolute Maximum Ratings

Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	-11	A
I_D @ $T_C = 100^\circ C$	-6.8	
I_{DM}	-44	
P_D @ $T_C = 25^\circ C$	125	W
Linear Derating Factor	1.0	W/°C
V_{GS}	± 20	V
E_{AS}	700	mJ
I_{AR}	-11	A
E_{AR}	13	mJ
dv/dt	-5.0	V/ns
T_J	-55 to +150	°C
T_{STG}		
Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
R_{JC}	—	—	1.0	°C/W
R_{CS}	—	0.50	—	
R_{JA}	—	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=-1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.50	Ω	$V_{GS}=-10V, I_D=-6.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}, I_D=-250\mu A$
g_{fs}	Forward Transconductance	4.1	—	—	S	$V_{DS}=-50V, I_D=-6.6A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	$V_{DS}=-200V, V_{GS}=0V$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-500	nA	$V_{DS}=-160V, V_{GS}=0V, T_J=125^\circ\text{C}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=20V$
Q_g	Total Gate Charge	—	—	44	nC	$V_{DS}=20V$
Q_{gs}	Gate-to-Source Charge	—	—	7.1		$I_D=-11A$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	27		$V_{DS}=160V$
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DS}=10V$ See Fig. 6 and 13 ④
t_r	Rise Time	—	43	—		$V_{DD}=-100V$
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		$I_D=-11A$
t_f	Fall Time	—	38	—		$R_G=9.1\Omega$
L_D	Internal Drain Inductance	—	4.5	—	nH	$R_D=8.6\Omega$ See Figure 10 ④
L_S	Internal Source Inductance	—	7.5	—		Between lead, 6 mm (0.25in.) from package and center of die contact
C_{iss}	Input Capacitance	—	1200	—	pF	$V_{DS}=0V$
C_{oss}	Output Capacitance	—	370	—		$V_{DS}=-25V$
C_{rss}	Reverse Transfer Capacitance	—	81	—		$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	$T_J=25^\circ\text{C}, I_S=-11A, V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	250	300	ns	$T_J=25^\circ\text{C}, I_F=-11A$
Q_{rr}	Reverse Recovery Charge	—	2.9	3.6	μC	$di/dt=100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=-50V$, starting $T_J=25^\circ\text{C}$, $L=8.7mH$, $R_G=25\Omega$, $I_{AS}=-11A$ (See Figure 12)
- ③ $I_{SDS}=11A$, $di/dt=150A/\mu s$, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

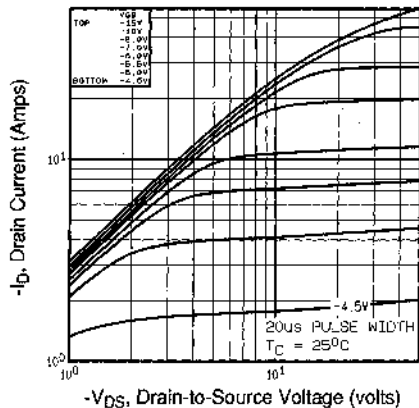


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

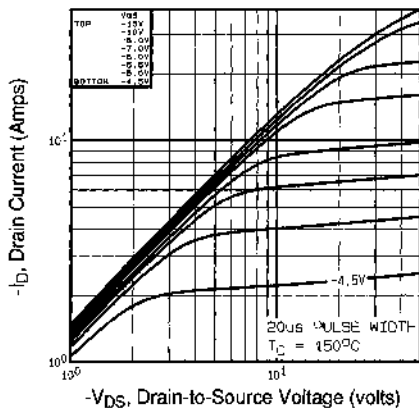


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

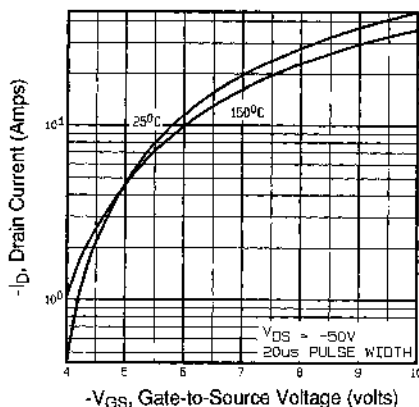


Fig 3. Typical Transfer Characteristics

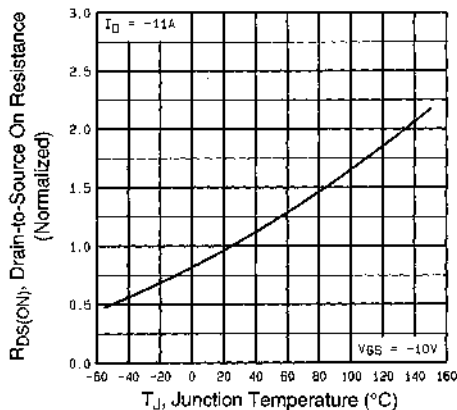


Fig 4. Normalized On-Resistance
Vs. Temperature

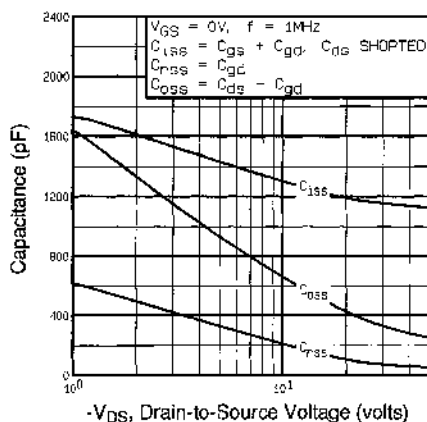


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

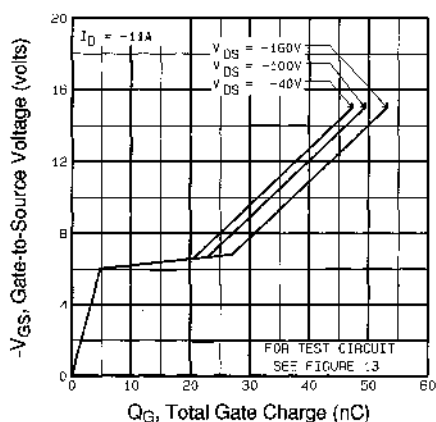


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

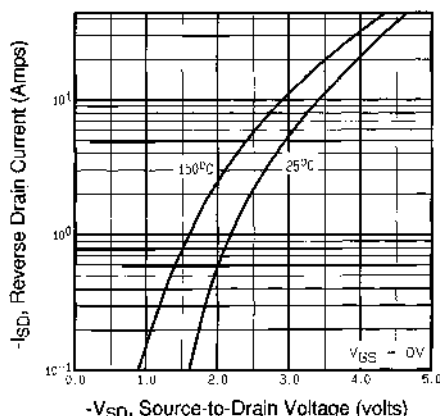


Fig 7. Typical Source-Drain Diode Forward Voltage

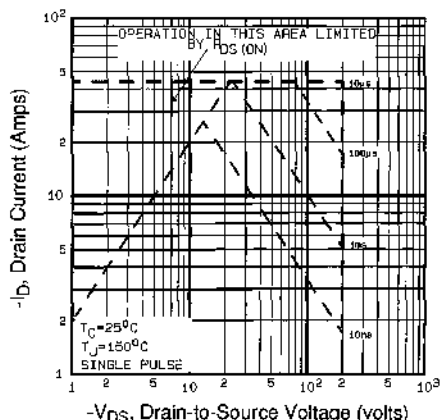


Fig 8. Maximum Safe Operating Area

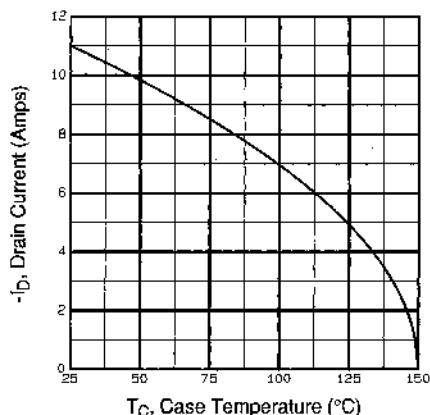


Fig 9. Maximum Drain Current Vs. Case Temperature

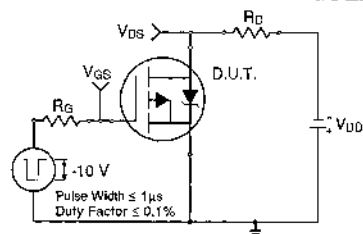


Fig 10a. Switching Time Test Circuit

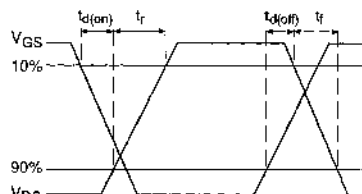


Fig 10b. Switching Time Waveforms

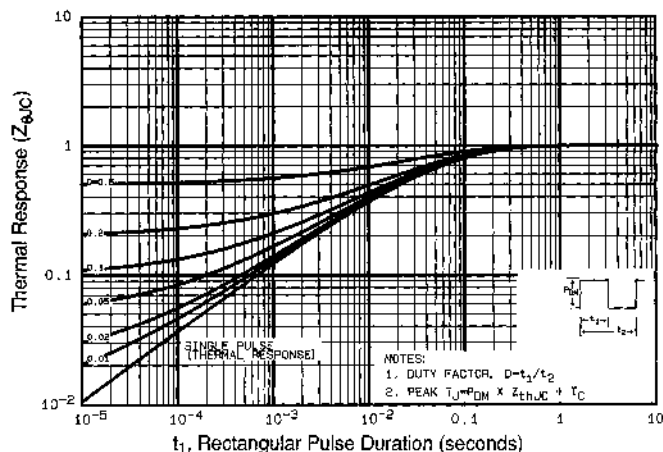


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

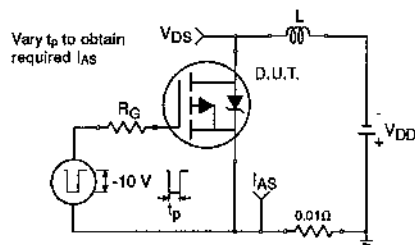


Fig 12a. Unclamped Inductive Test Circuit

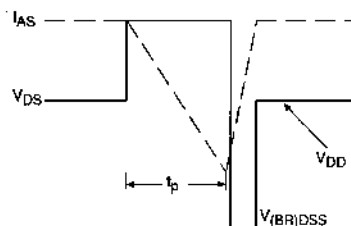


Fig 12b. Unclamped Inductive Waveforms

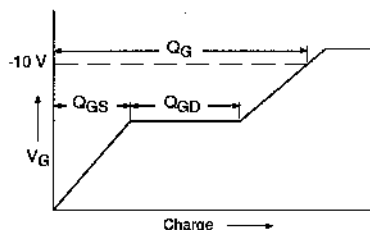


Fig 13a. Basic Gate Charge Waveform

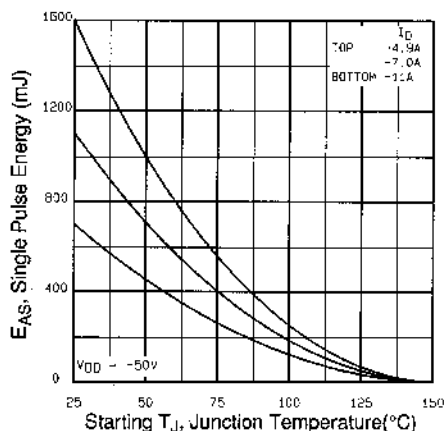


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

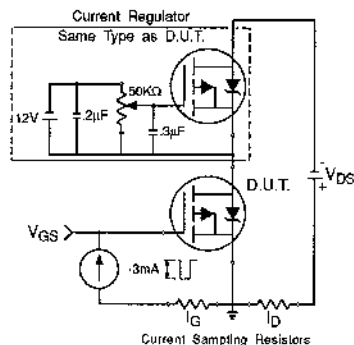


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

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