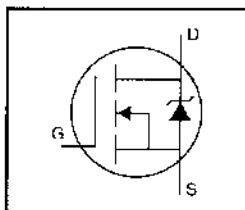


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}=4V$ & $5V$
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 200V$$

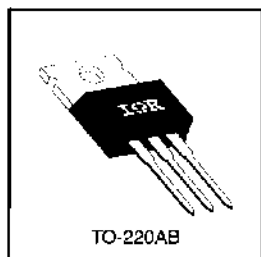
$$R_{DS(on)} = 0.18\Omega$$

$$I_D = 17A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$ Continuous Drain Current, $V_{GS} @ 5.0V$	17	A
I_D @ $T_C = 100^\circ C$ Continuous Drain Current, $V_{GS} @ 5.0V$	11	
I_{DM} Pulsed Drain Current ①	68	
P_D @ $T_C = 25^\circ C$ Power Dissipation	125	W
Linear Derating Factor	1.0	W/°C
V_{GS} Gate-to-Source Voltage	± 10	V
E_{AS} Single Pulse Avalanche Energy ②	580	mJ
I_{AS} Avalanche Current ③	10	A
E_{AR} Repetitive Avalanche Energy ④	13	mJ
dv/dt Peak Diode Recovery dv/dt ⑤	5.0	V/ns
T_J Operating Junction and Storage Temperature Range	-55 to +150	°C
Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
Mounting Torque, 6-32 or M3 screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
R_{JC} Junction-to-Case	—	—	1.0	°C/W
R_{JCS} Case-to-Sink, Flat, Greased Surface	—	0.50	—	
R_{JA} Junction-to-Ambient	—	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	$V_{GS}=5.0V$, $I_D=10A$ ②
		—	—	0.27		$V_{DS}=4.0V$, $I_D=8.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS}=50V$, $I_D=10A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=200V$, $V_{GS}=0V$
		—	—	250		$V_{DS}=160V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
Q_g	Total Gate Charge	—	—	66	nC	$I_D=17A$
Q_{gs}	Gate-to-Source Charge	—	—	9.0		$V_{DS}=160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38		$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	$V_{DS}=100V$
t_r	Rise Time	—	83	—		$I_D=17A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G=4.6\Omega$
t_f	Fall Time	—	52	—		$R_D=5.7\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1800	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	400	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—		$f=1.0MHz$ See Figure 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	68		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=17A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	310	470	ns	$T_J=25^\circ\text{C}$, $I_F=17A$
Q_{rr}	Reverse Recovery Charge	—	3.2	4.8	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

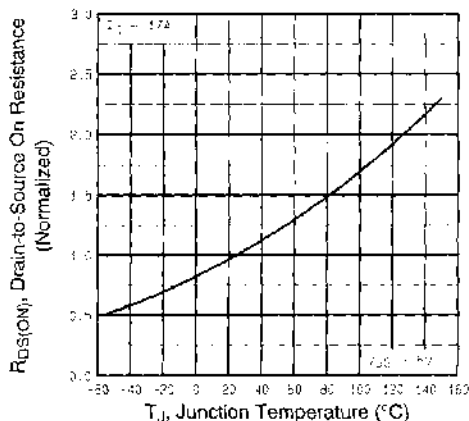
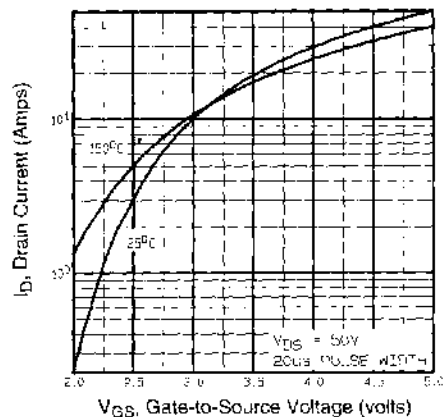
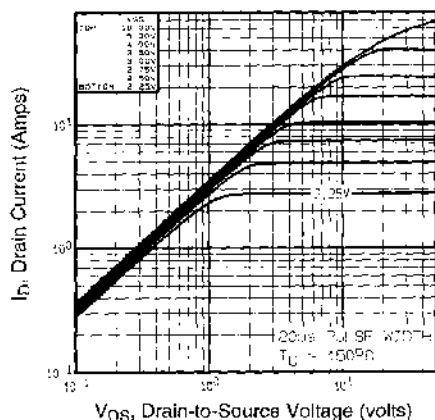
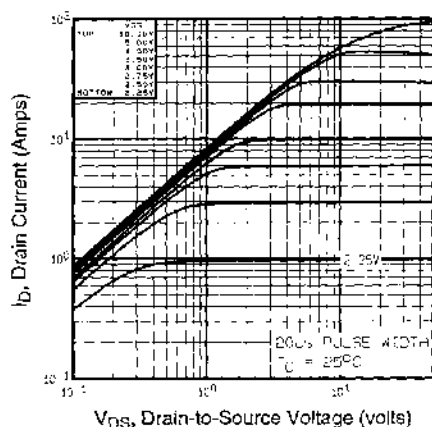
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $I_{SDS} \leq 17A$, $di/dt \leq 150A/\mu s$, $V_{DSS} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

③ $V_{DS}=50V$, starting $T_J=25^\circ\text{C}$, $L=3.0mH$, $R_G=25\Omega$, $I_{AS}=17A$ (See Figure 12)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



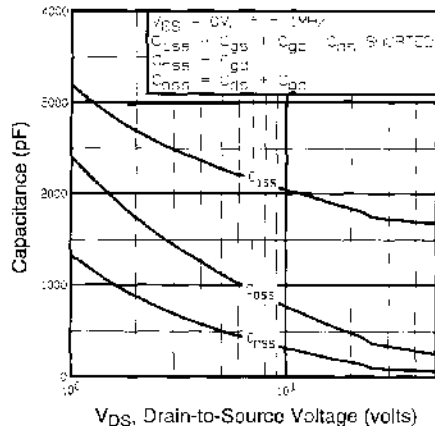


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

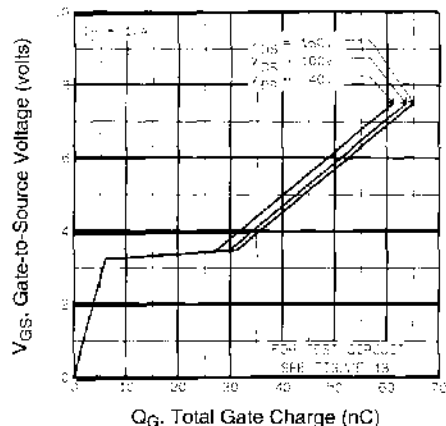


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

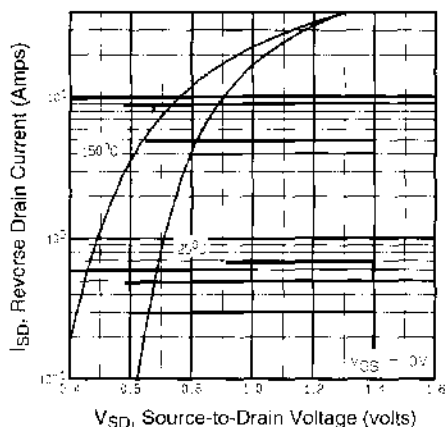


Fig 7. Typical Source-Drain Diode Forward Voltage

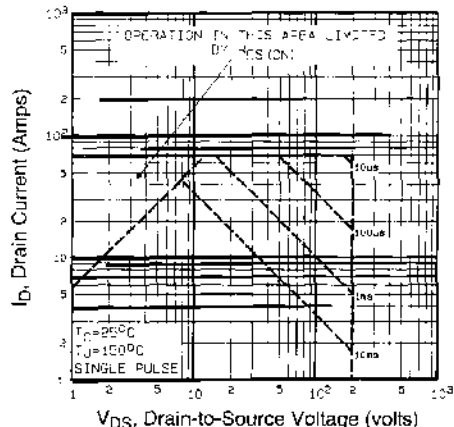


Fig 8. Maximum Safe Operating Area

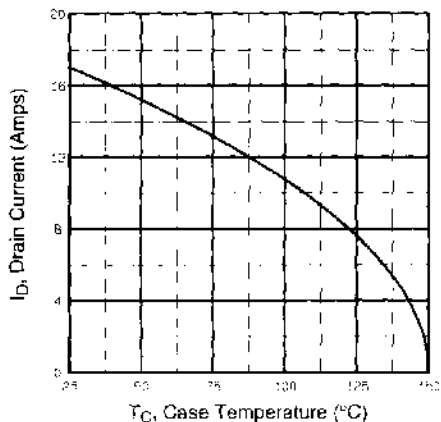


Fig 9. Maximum Drain Current Vs. Case Temperature

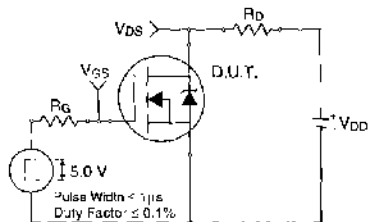


Fig 10a. Switching Time Test Circuit

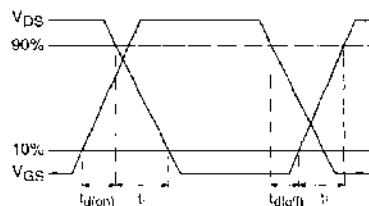


Fig 10b. Switching Time Waveforms

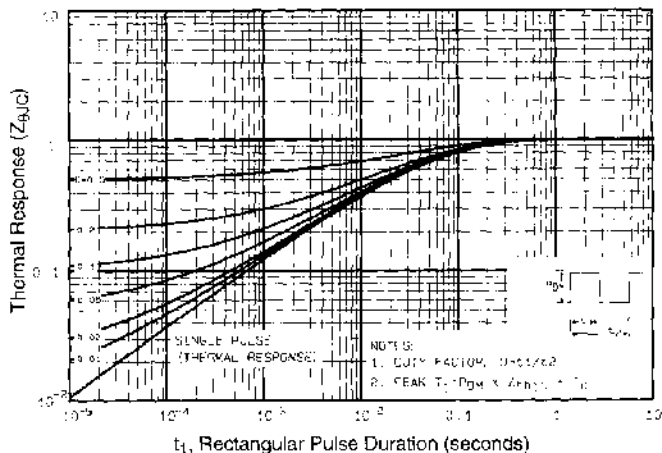


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

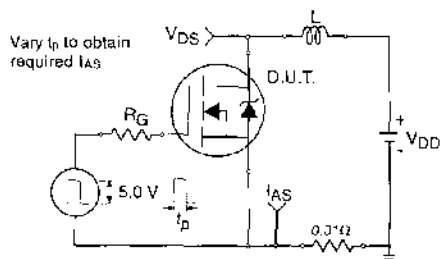


Fig 12a. Unclamped Inductive Test Circuit

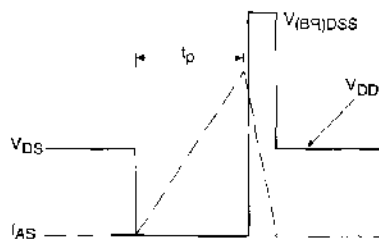


Fig 12b. Unclamped Inductive Waveforms

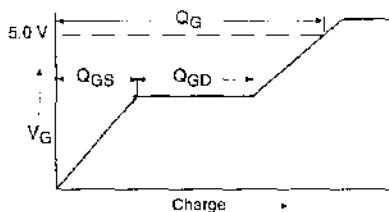


Fig 13a. Basic Gate Charge Waveform

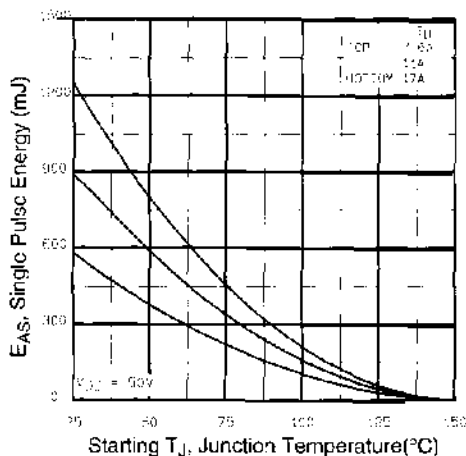


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

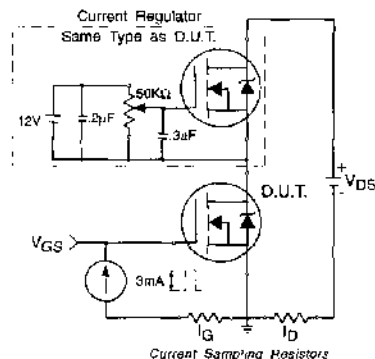


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

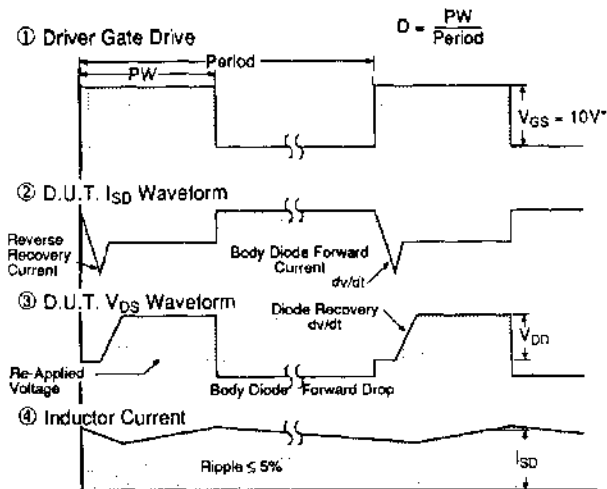
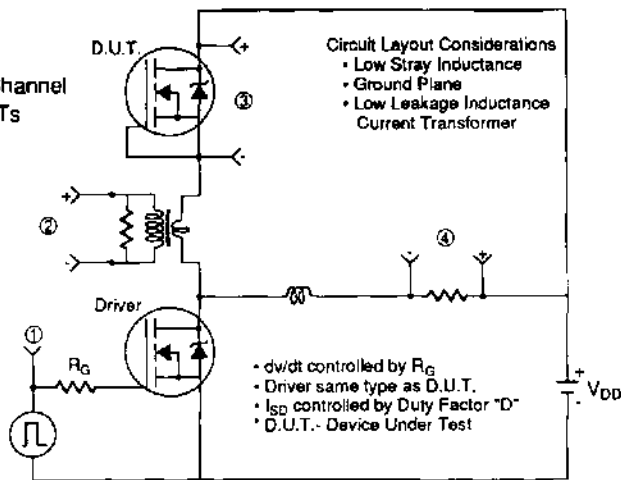
Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



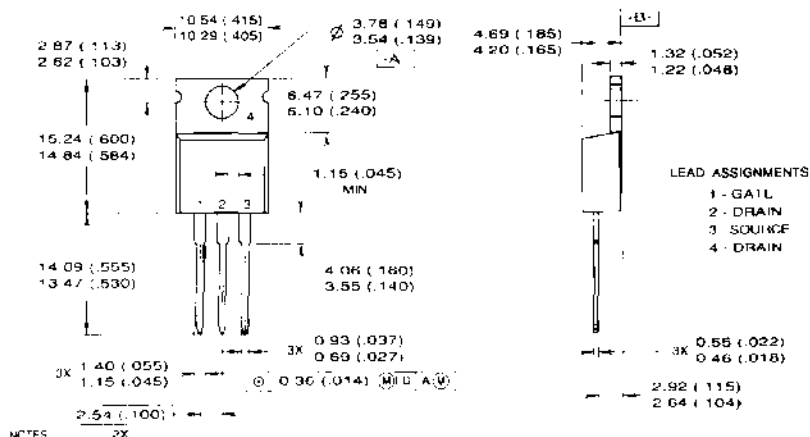
* $V_{GS} = 5V$ for Logic Level Devices

Package Outline

Appendix B

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982
- 2 CONTROLLING DIMENSION: NCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO 220 AB
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

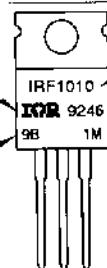
Part Marking Information

Appendix C

TO-220AB

EXAMPLE: THIS IS AN IRF1010 WITH
ASSEMBLY LOT CODE 9B1M

INTERNATIONAL
RECTIFIER
LOGO
ASSEMBLY
LOT CODE



PART NUMBER

DATE CODE
(YYWW)
YY = YEAR
WW = WEEK



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